

MV2 Build

	EE	DATE	POWER	DATE	INVENTEC			
DRAWER								
DESIGN					TITLE ABSOLUT			
CHECK								
RESPONSIBLE								
SIZE = 3								
FILE NAME : XXXX-XXXX-XX					VER :			
P/N : XXXXXXXXXX					SIZE A3 CODE CS DOC NUMBER <i>Model No</i> REV <i>A04</i>			
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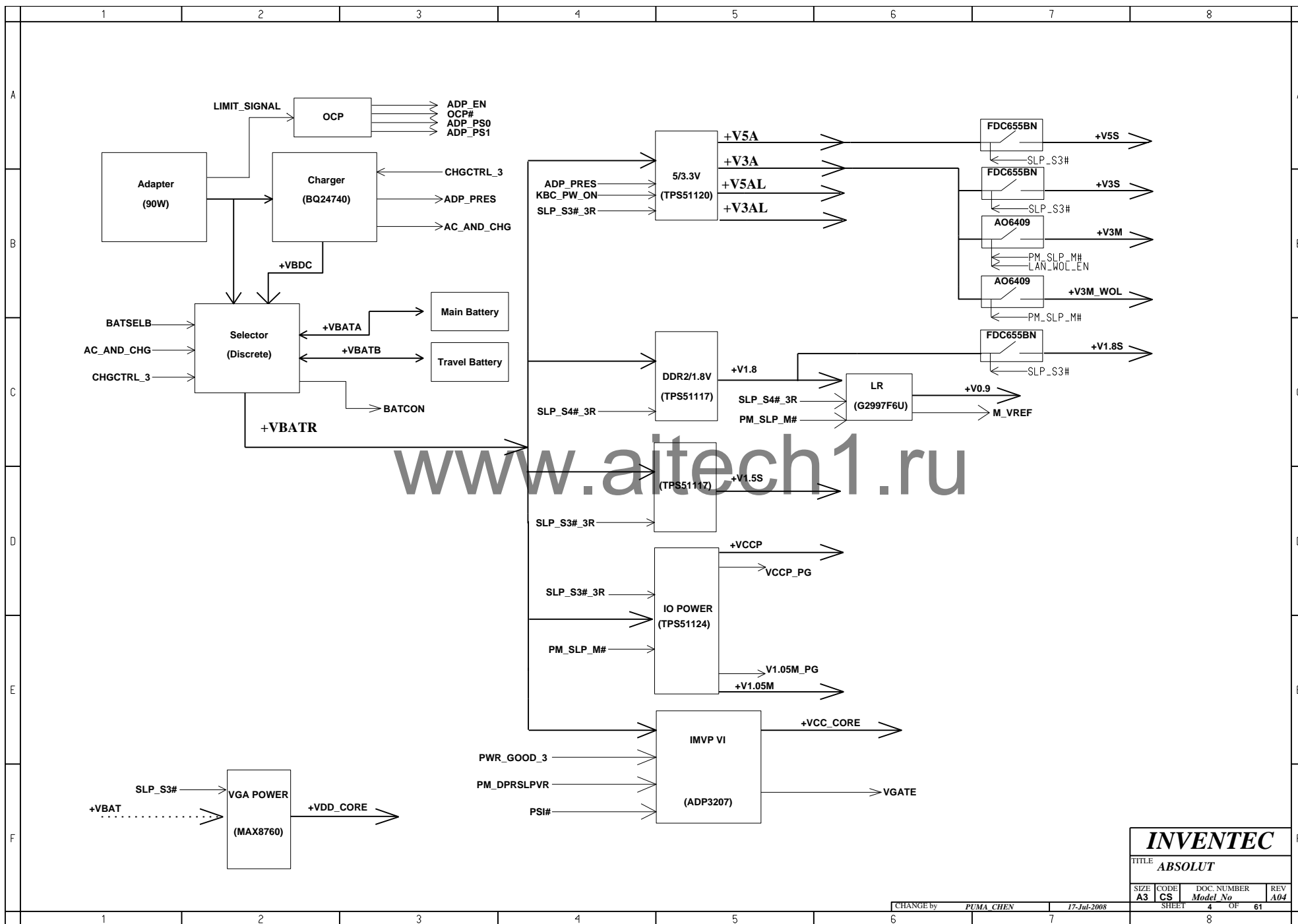
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TITLE **ABSOLUT**

SIZE A3	CODE CS	DOC. NUMBER <i>Model No</i>	REV A04
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CHANGE by **PUMA CHEN** 17-Jul-2008

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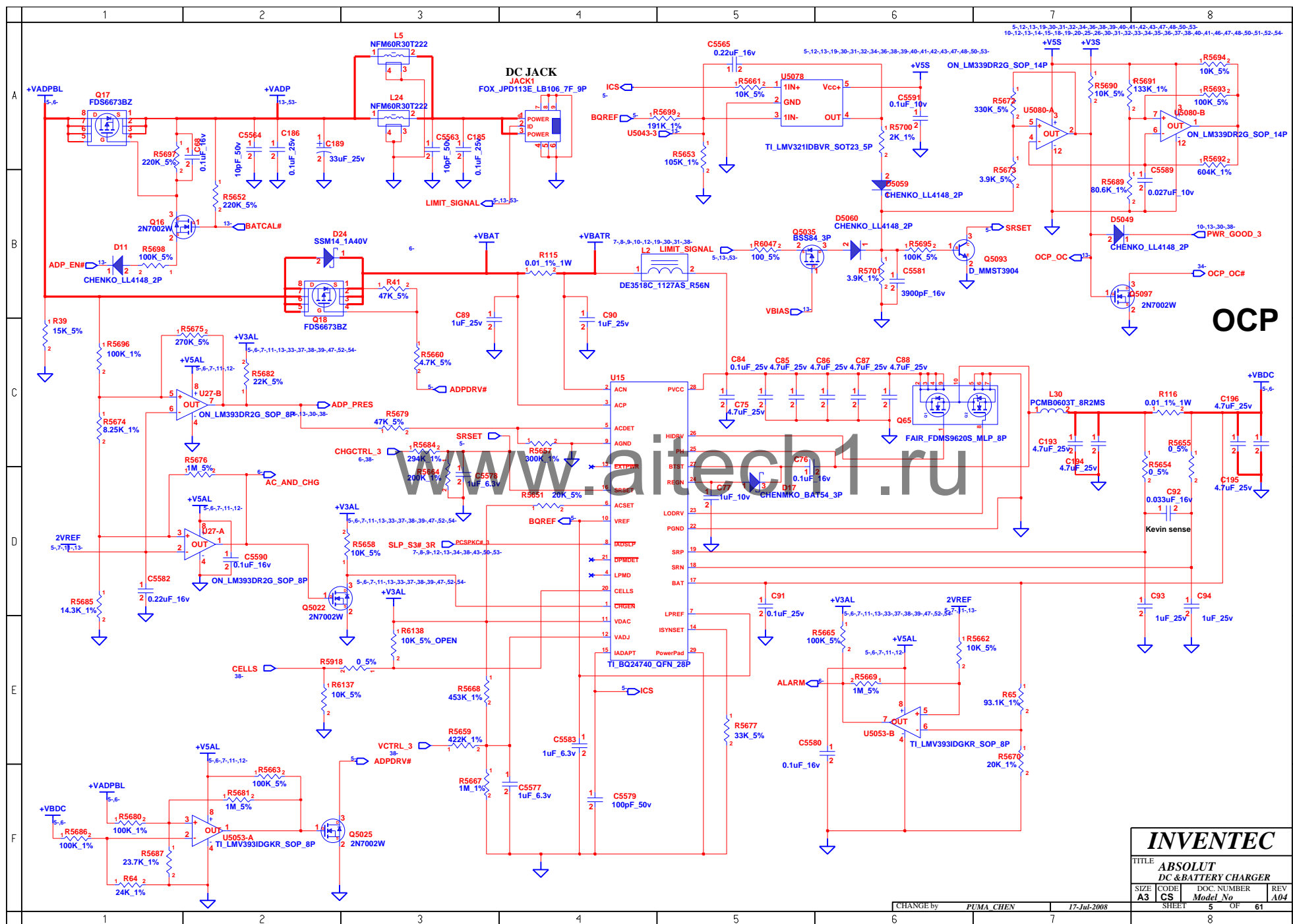
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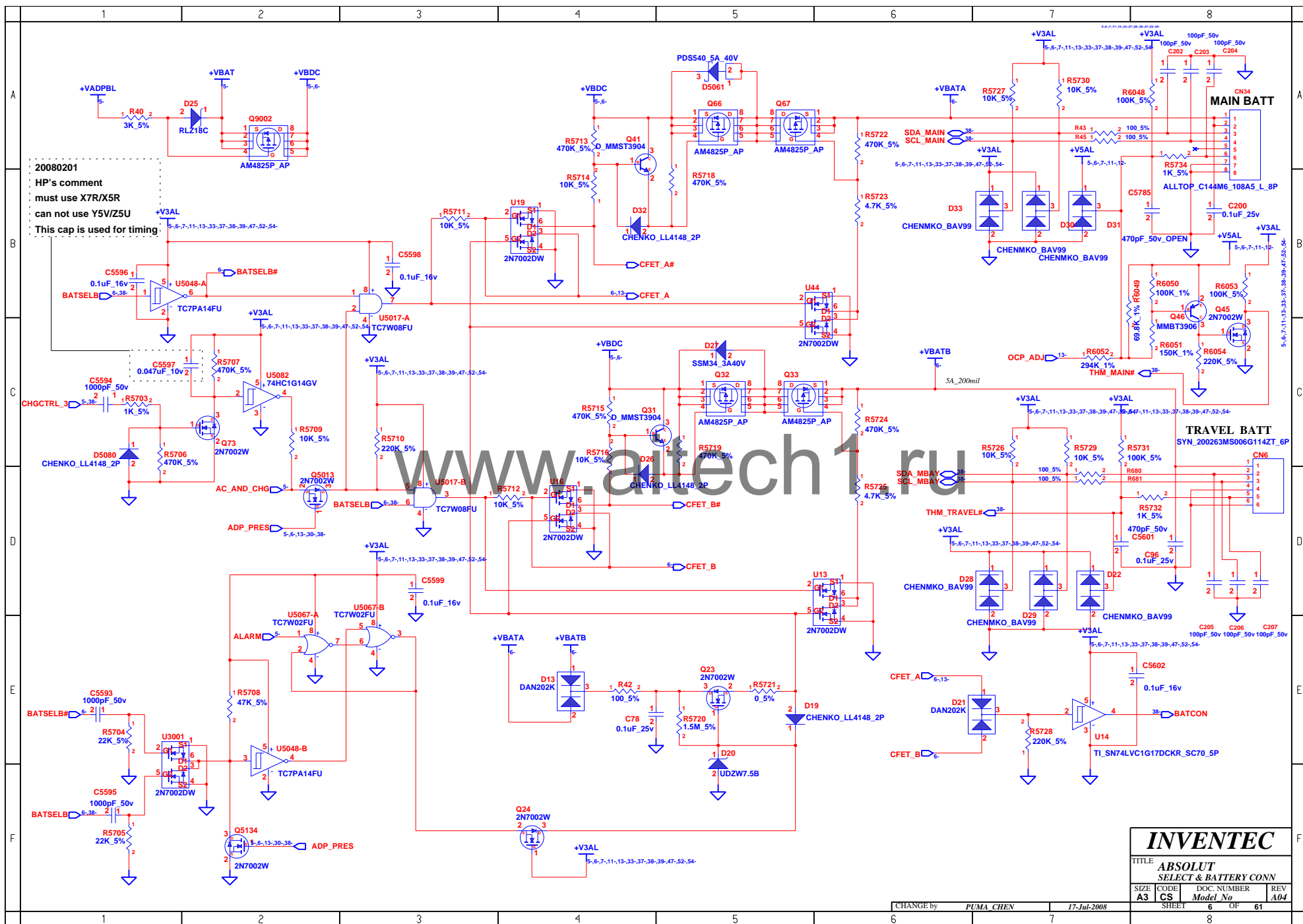
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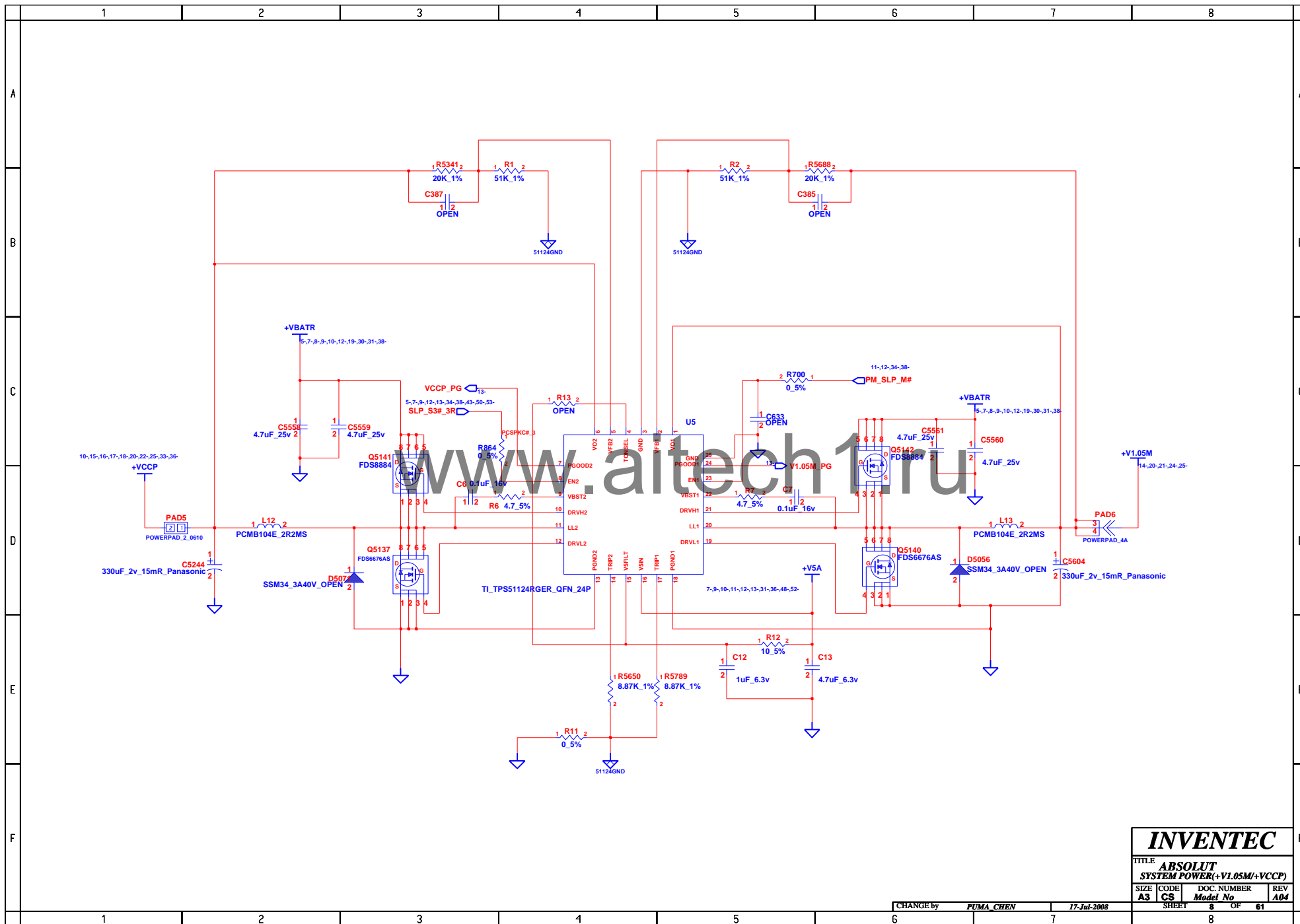
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A3	CS	Model No	A04

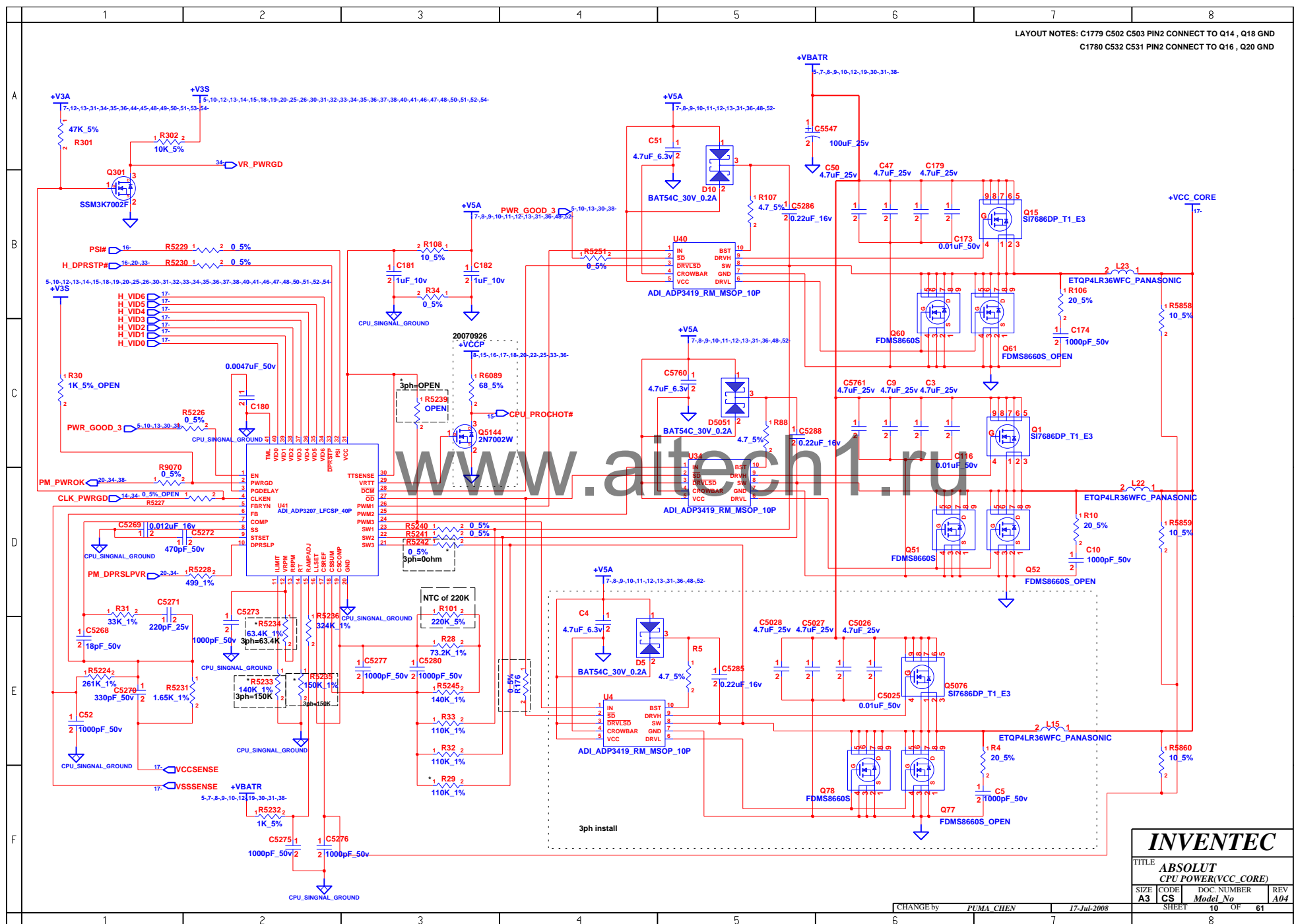
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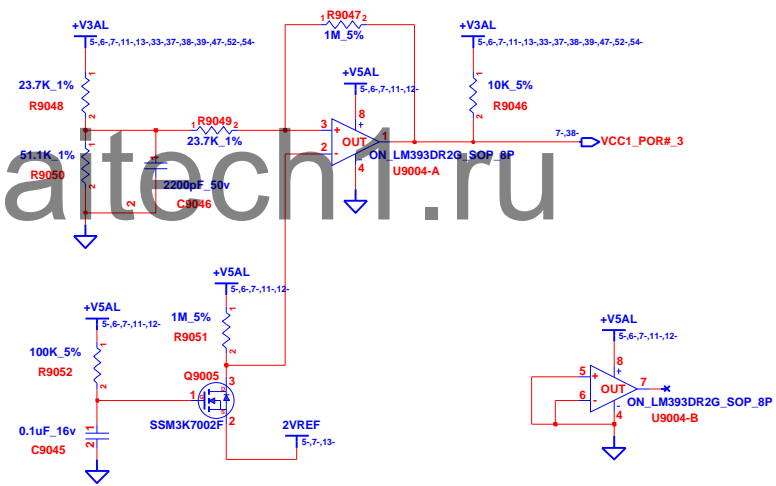
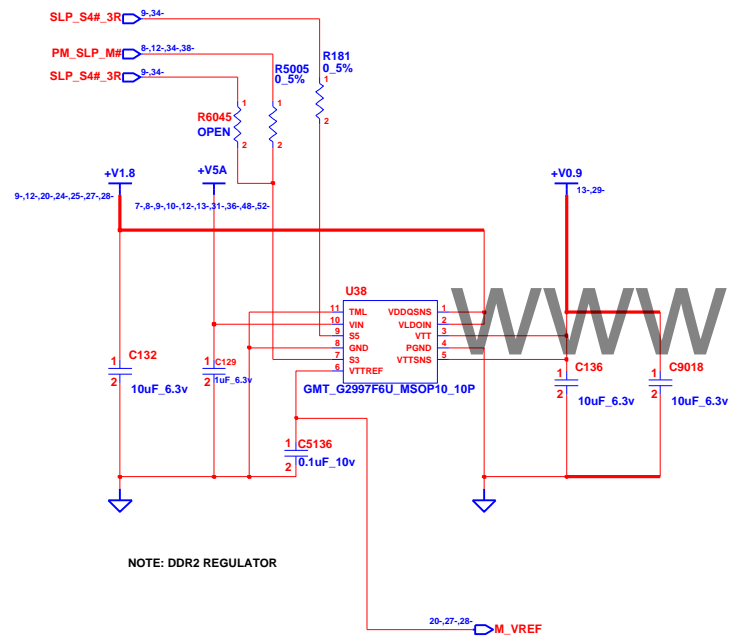
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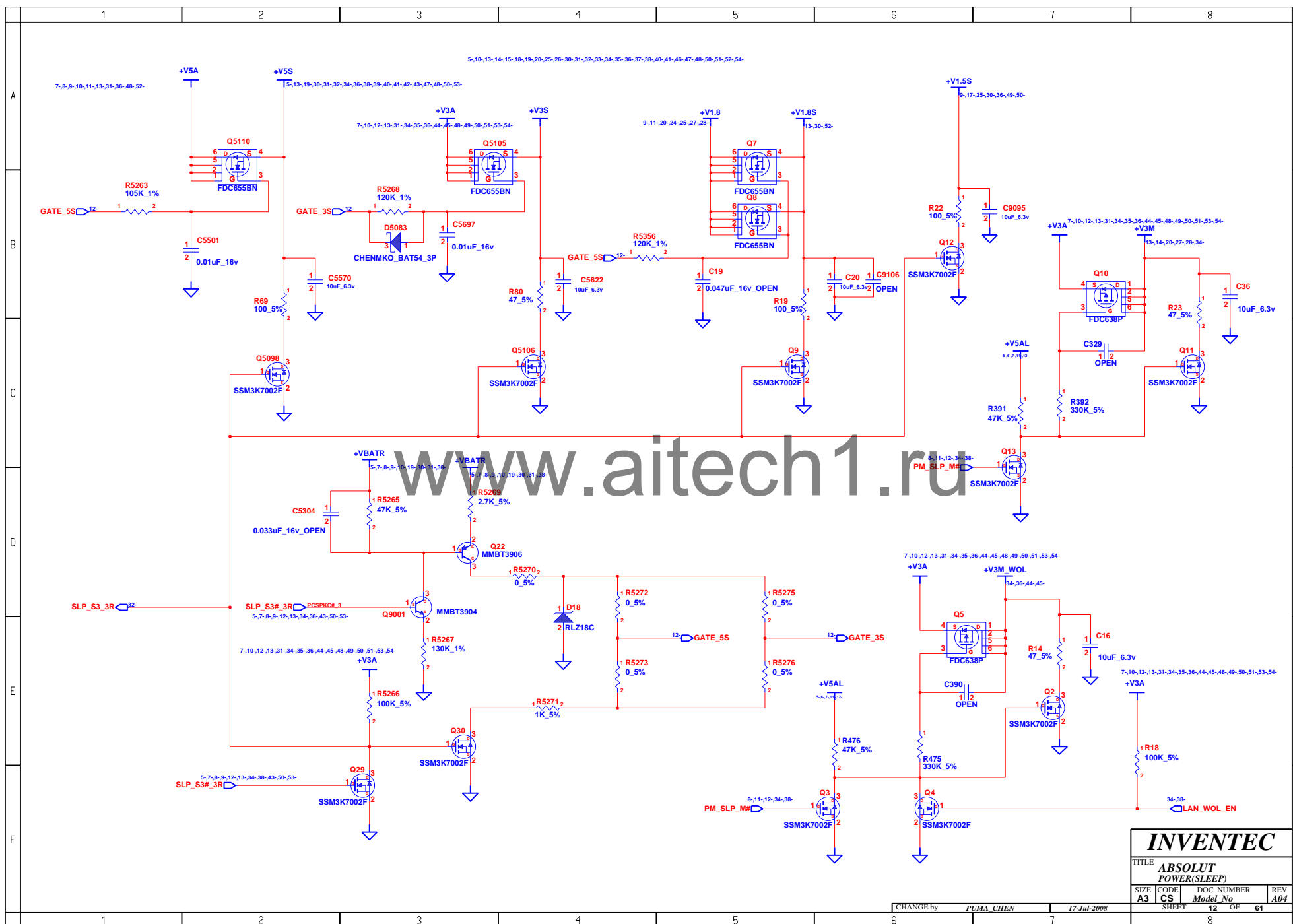


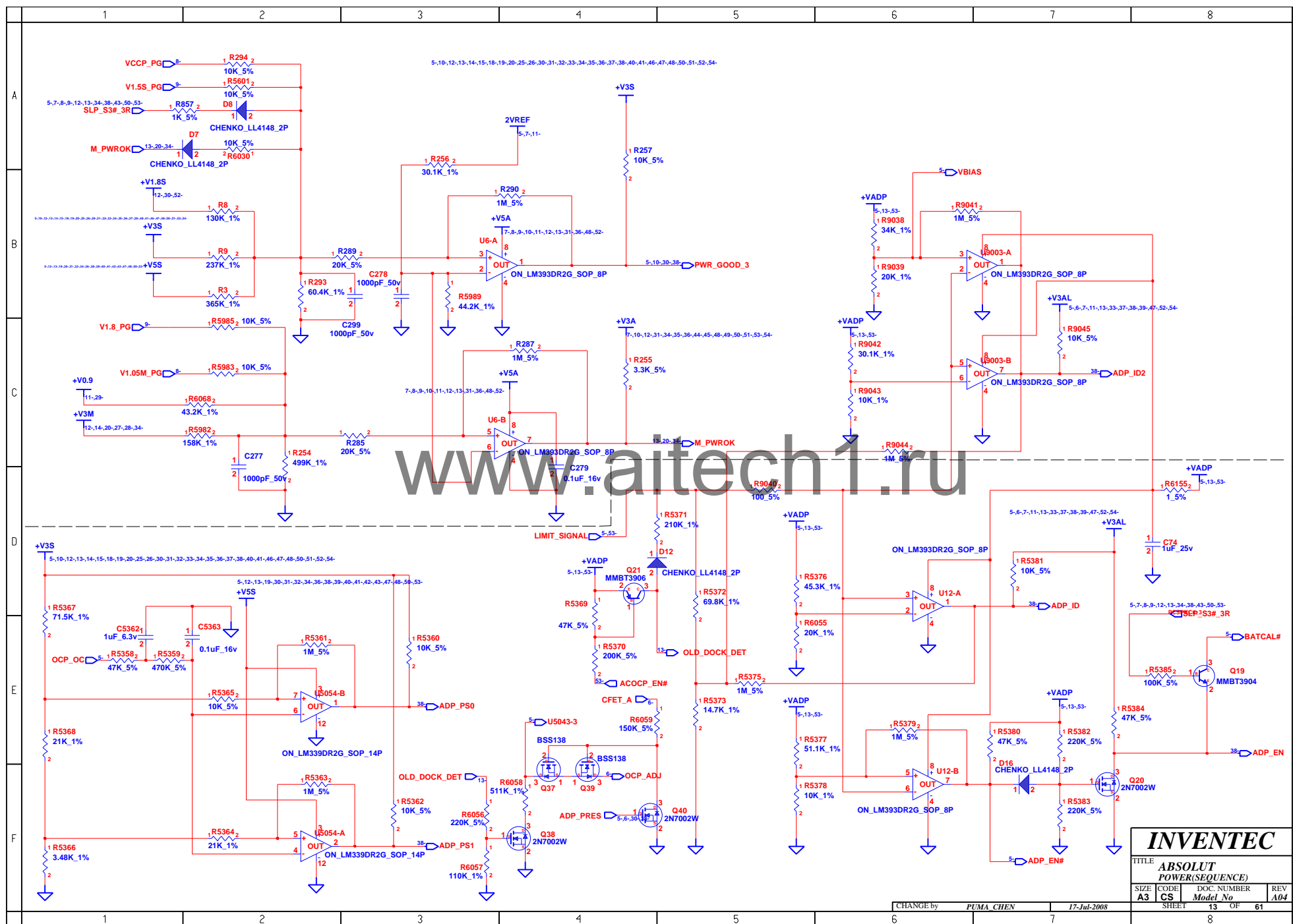


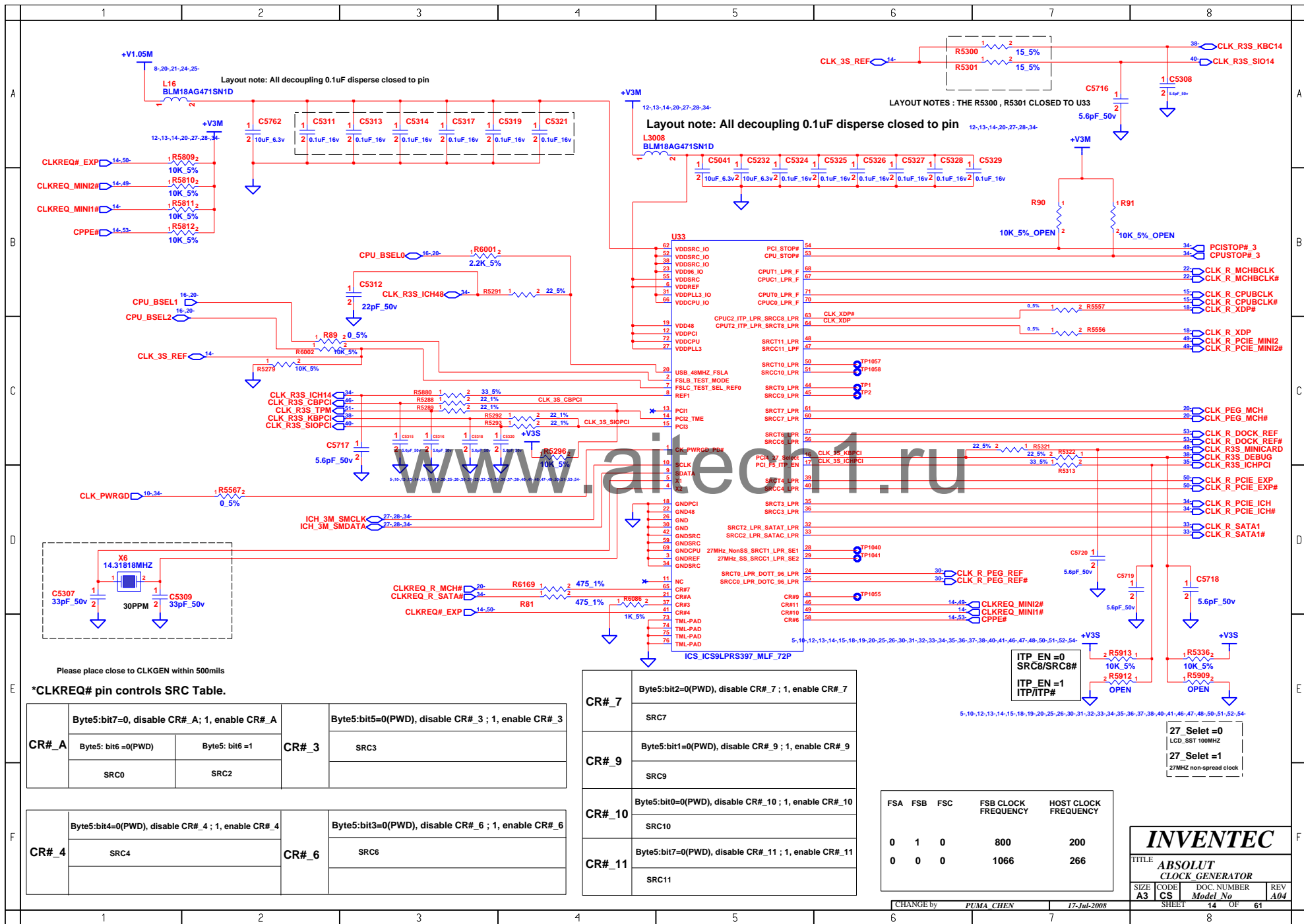




INVENTEC			
TITLE ABSOLUT DDR TERMINATION VOLTAGE			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV A04
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Please place close to CLKGEN within 500mils

*CLKREQ# pin controls SRC Table.

CR#_A	Byte5:bit7=0, disable CR#_A; 1, enable CR#_A		CR#_3	Byte5:bit5=0(PWD), disable CR#_3 ; 1, enable CR#_3	
	Byte5: bit6 =0(PWD)	Byte5: bit6 =1		SRC3	
	SRC0	SRC2			

CR#_4	Byte5:bit4=0(PWD), disable CR#_4 ; 1, enable CR#_4		CR#_6	Byte5:bit3=0(PWD), disable CR#_6 ; 1, enable CR#_6	
	SRC4			SRC6	

CR#_7	Byte5:bit2=0(PWD), disable CR#_7; 1, enable CR#_7
SRC7	

CR#_9	Byte5:bit1=0(PWD), disable CR#_9; 1, enable CR#_9
SRC9	

CR#_10	Byte5:bit0=0(PWD), disable CR#_10; 1, enable CR#_10
SRC10	

CR#_11	Byte5:bit7=0(PWD), disable CR#_11; 1, enable CR#_11
SRC11	

FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
0	1	0	800	200
0	0	0	1066	266

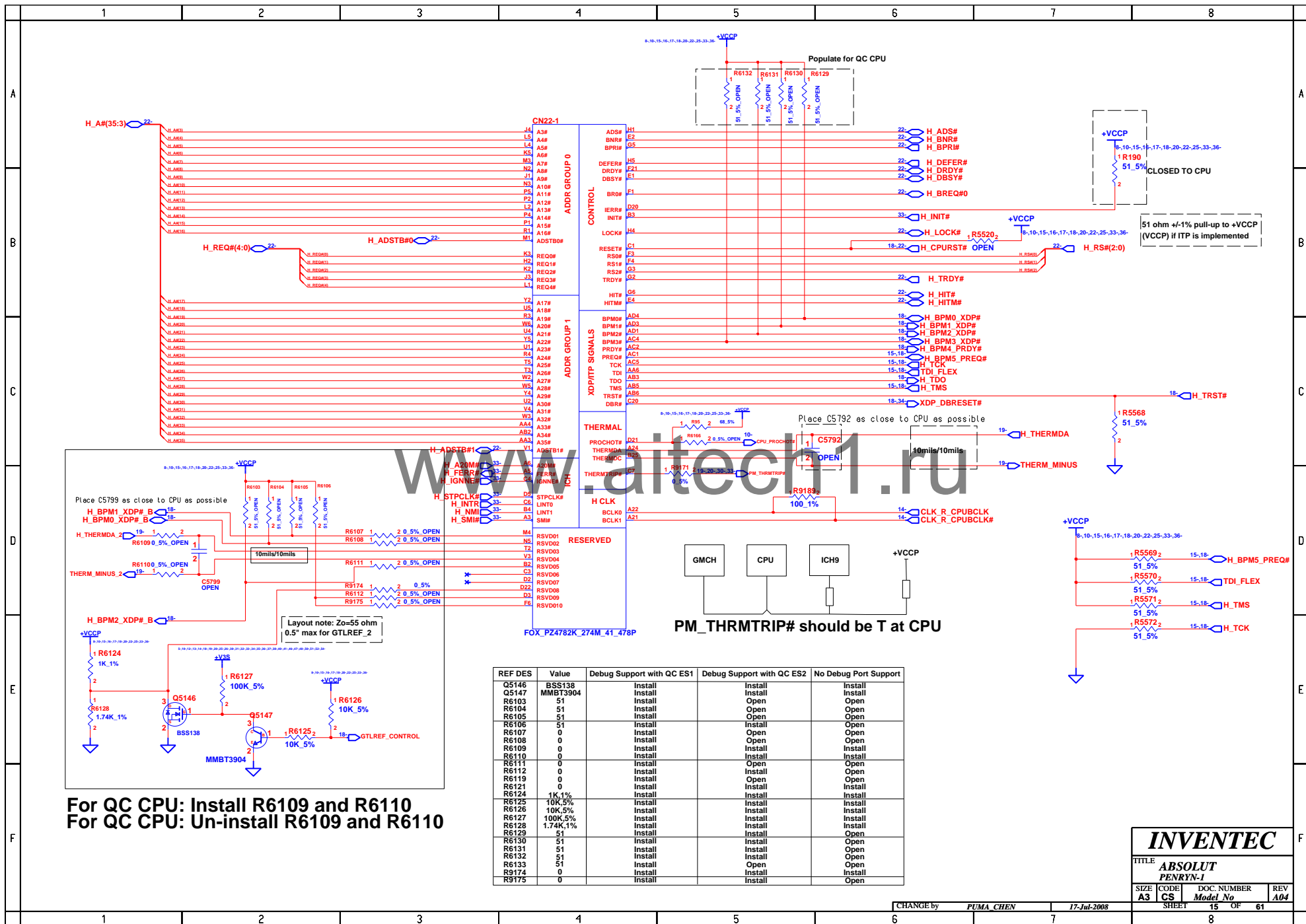
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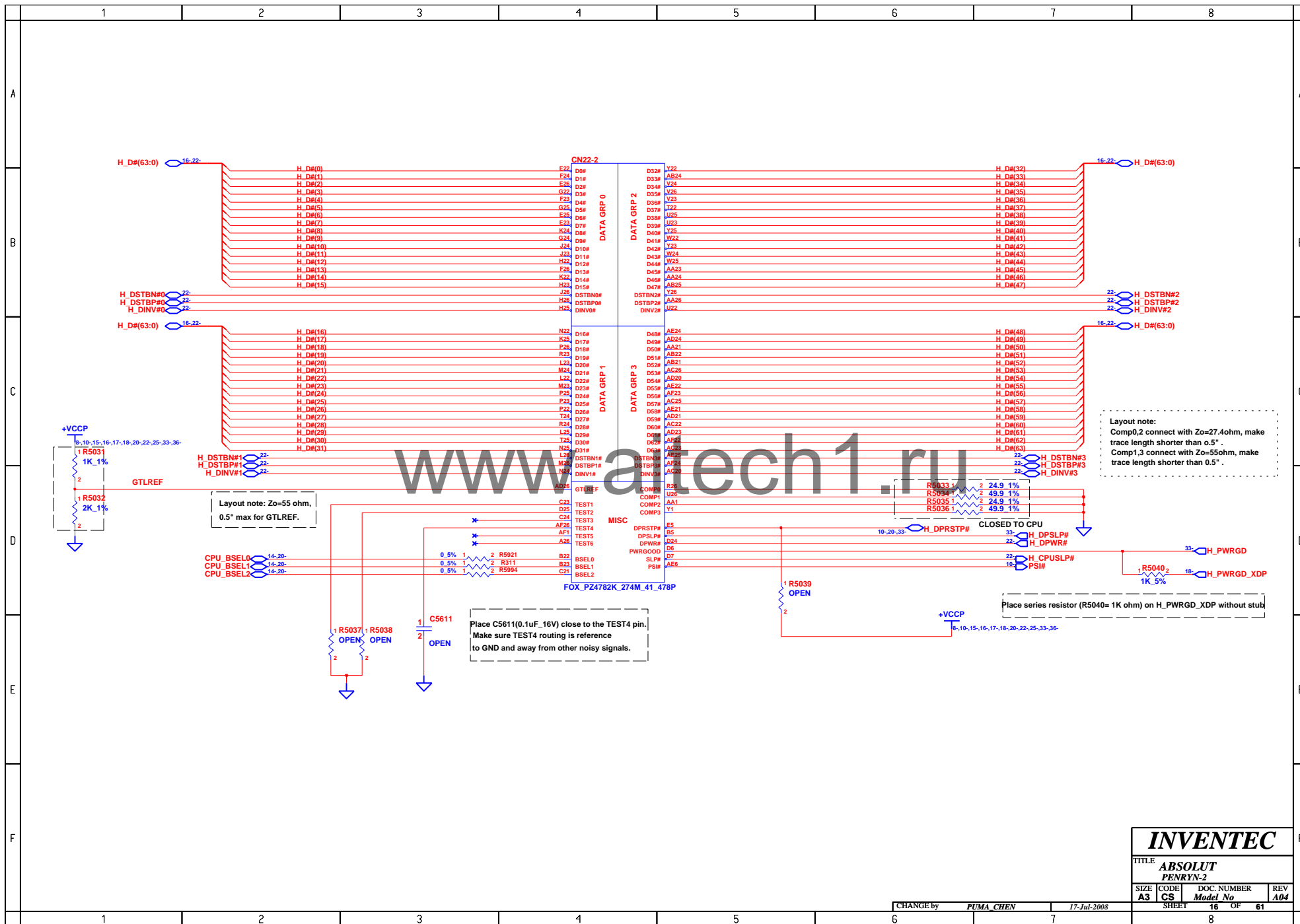
TITLE: **ABSOLUT**
CLOCK GENERATOR

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	A04

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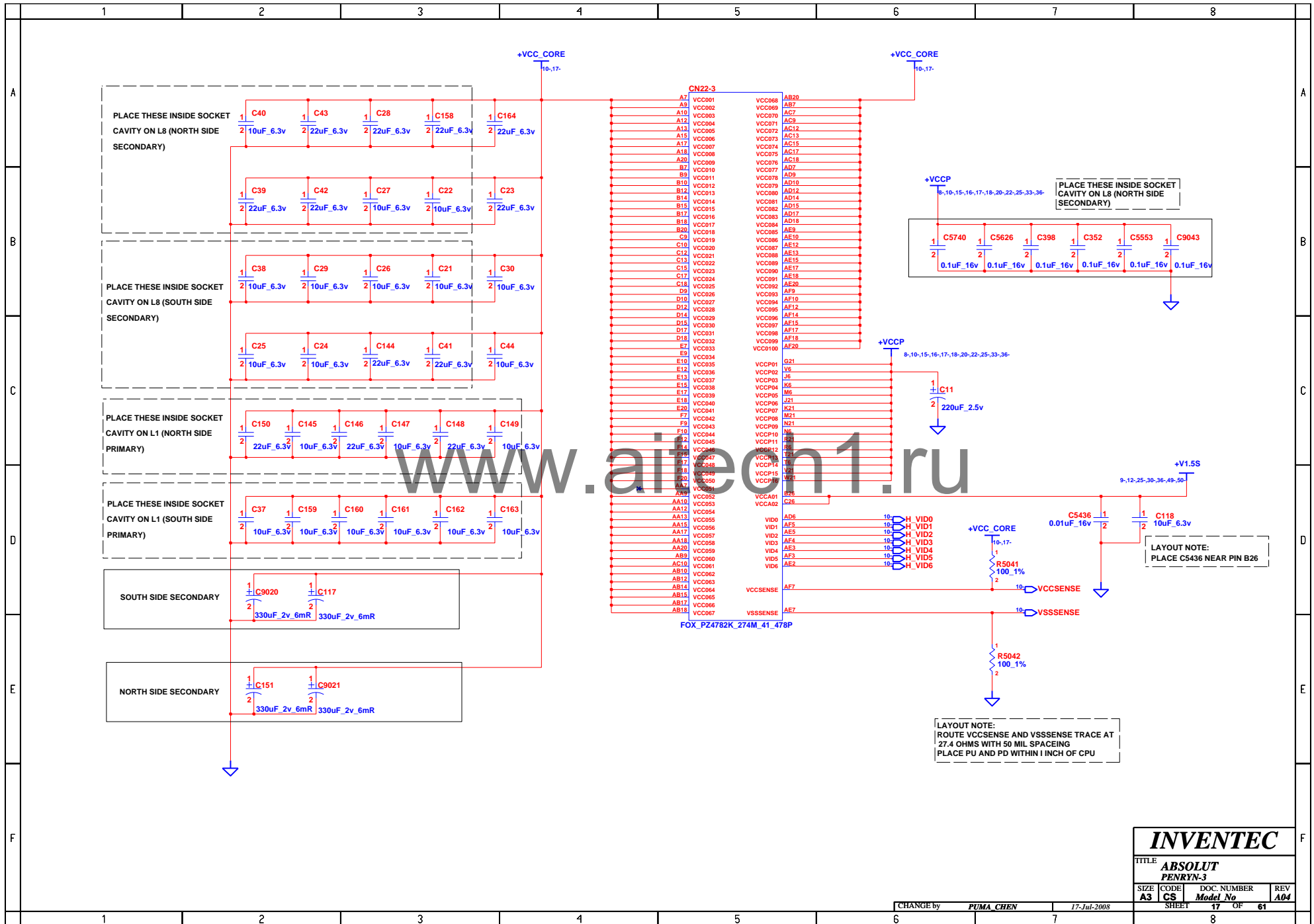


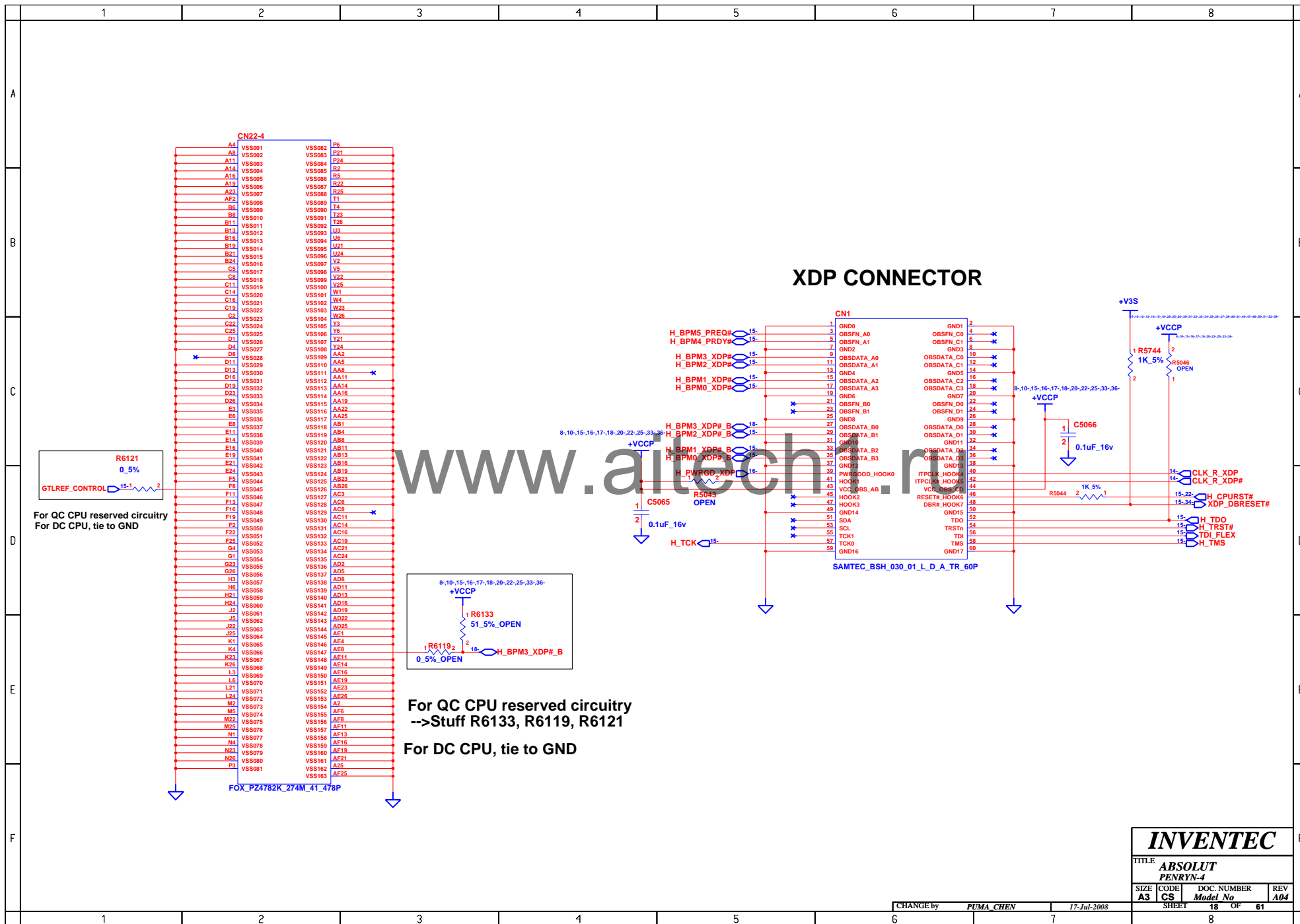


INVENTEC

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SIZE A3	CODE CS	DOC. NUMBER Model No	REV A04
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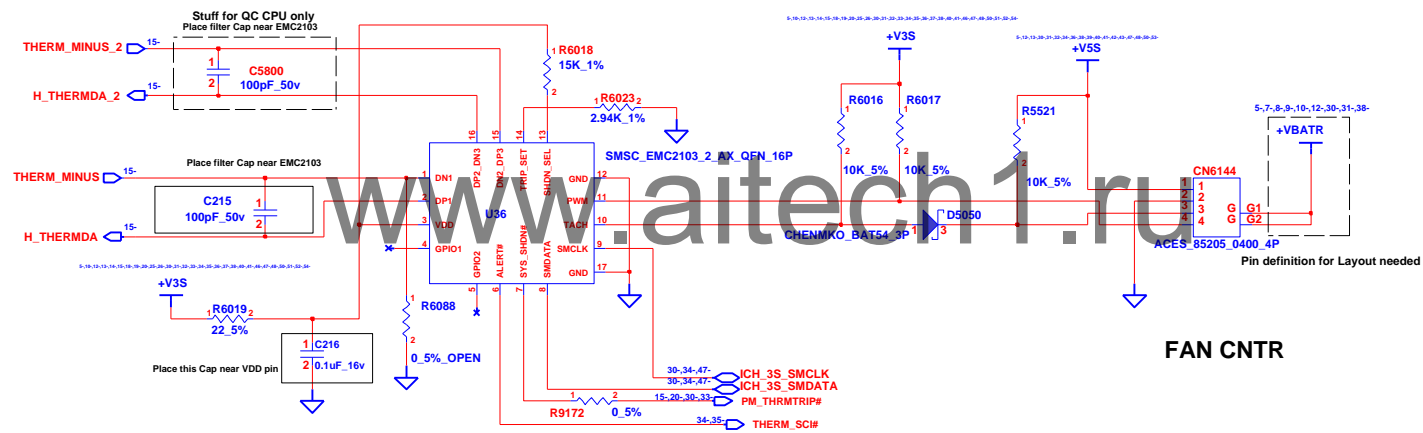
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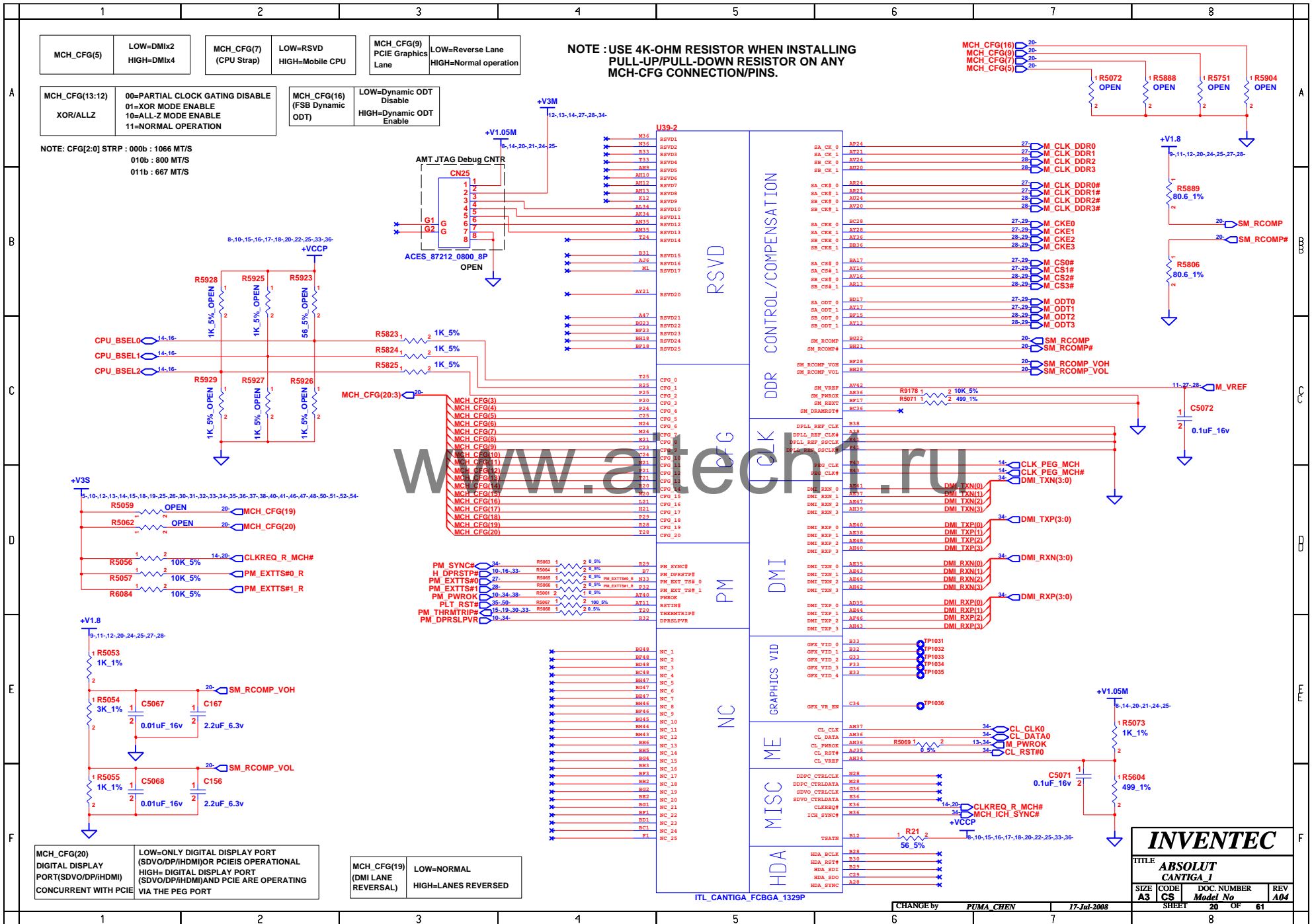
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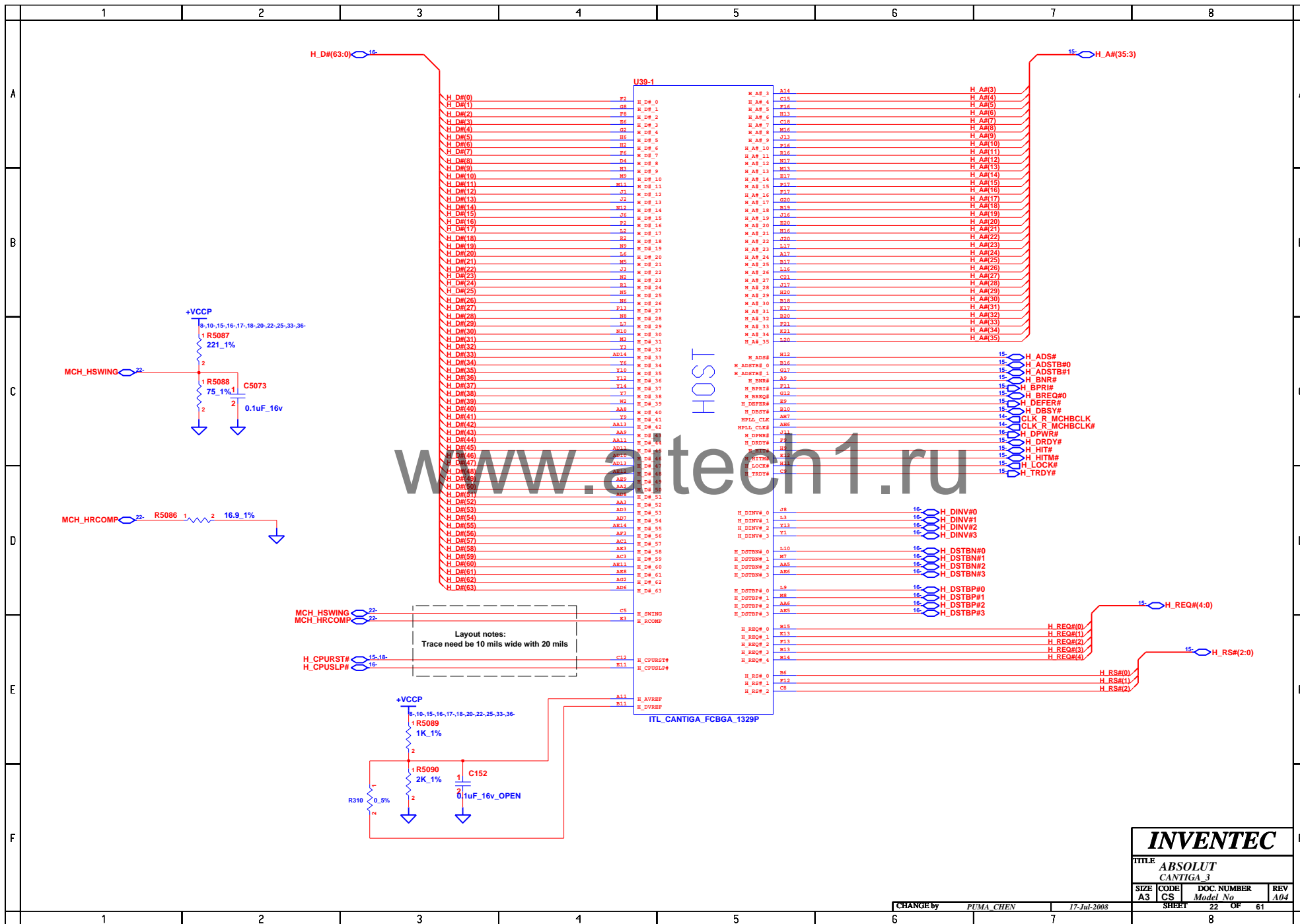
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LAYOUT NOTES: PUT THE THERMAL SENSOR CLOSE TO CPU

INVENTEC			
TITLE ABSOLUT THERMAL&FAN CONTROLLER			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV A04
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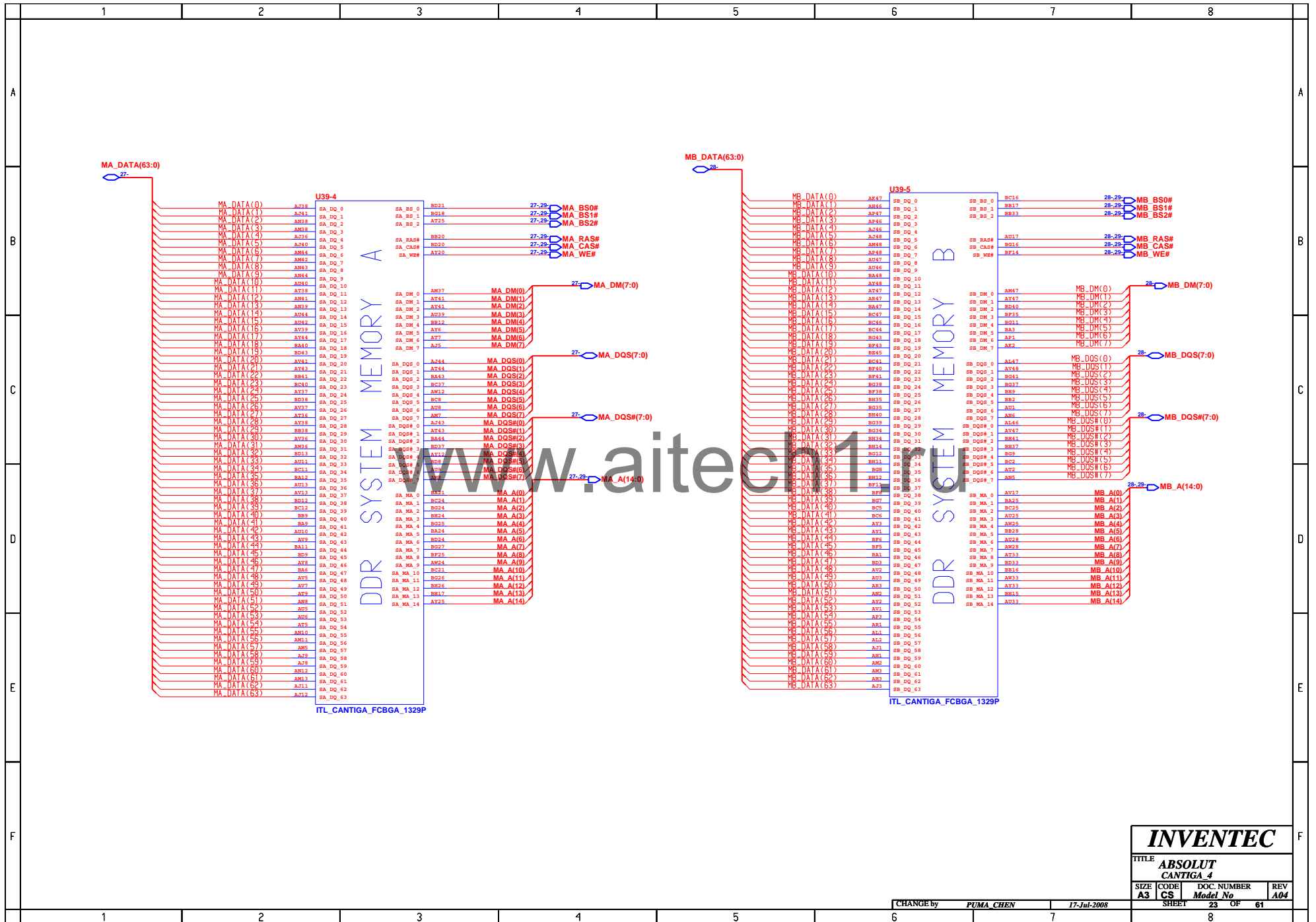
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TITLE
ABSOLUT
CANTIGA 3

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	A04

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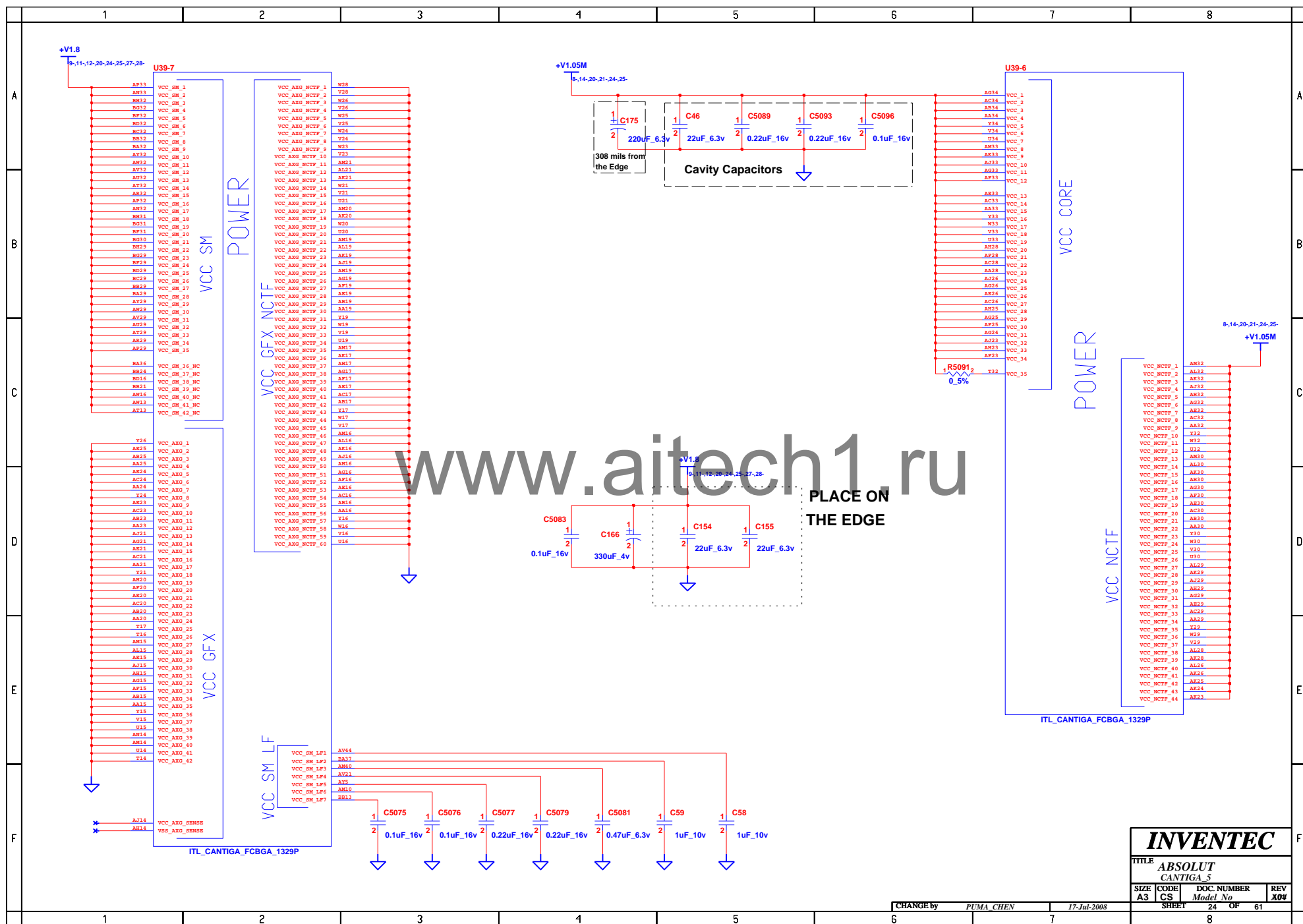
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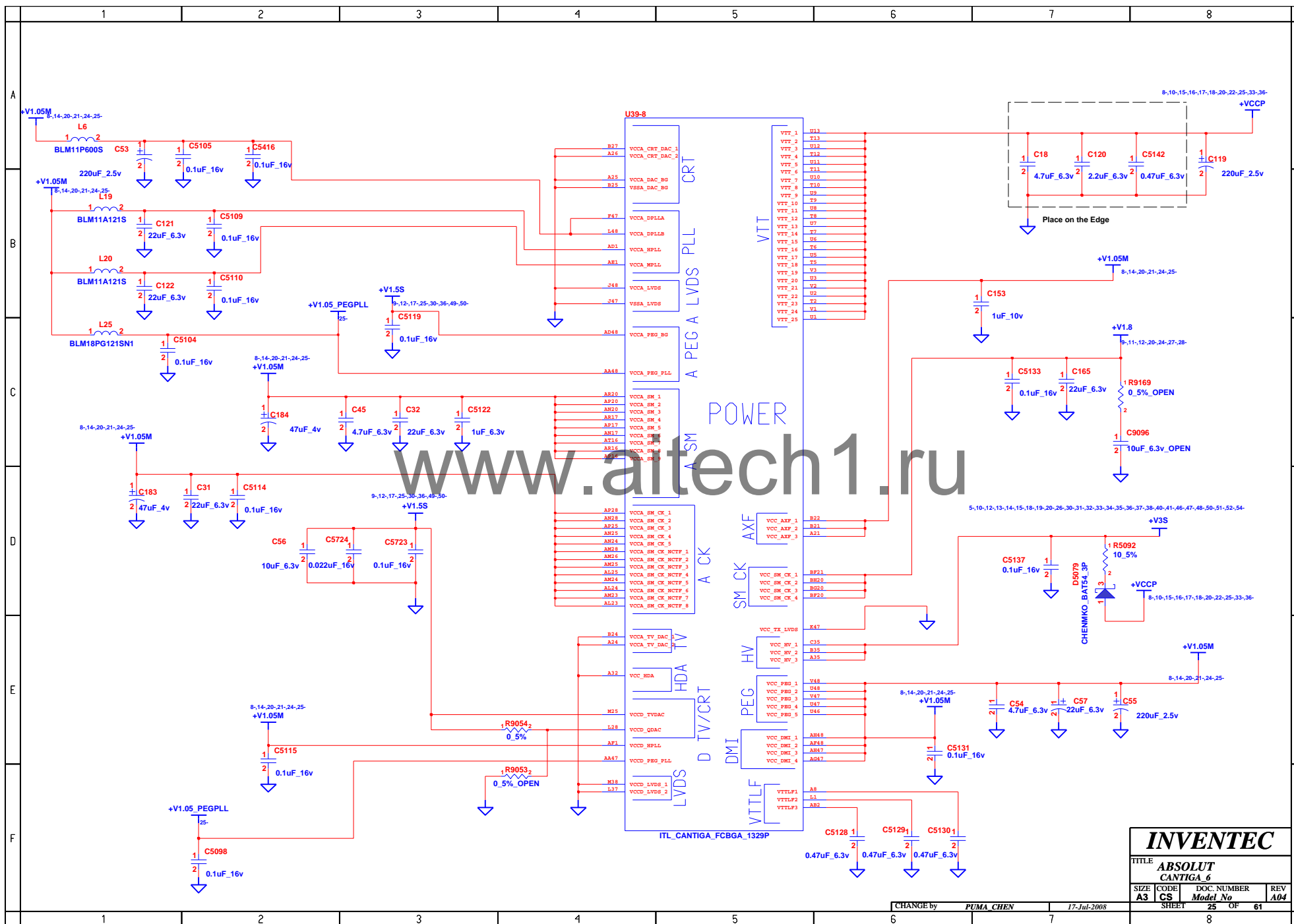
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**ABSOLUT
CANTIGA 4**

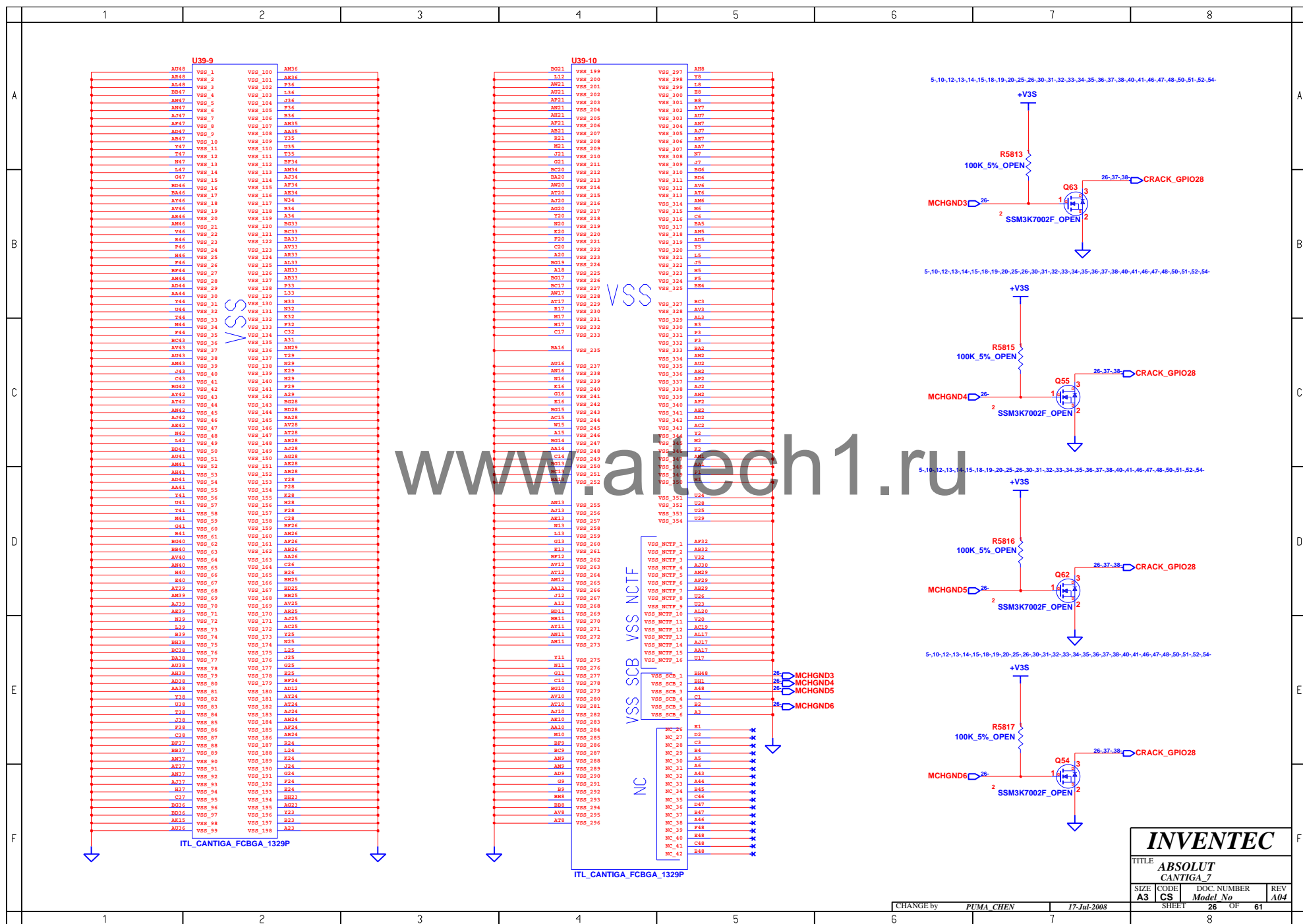
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A3	CS	Model No.	A04

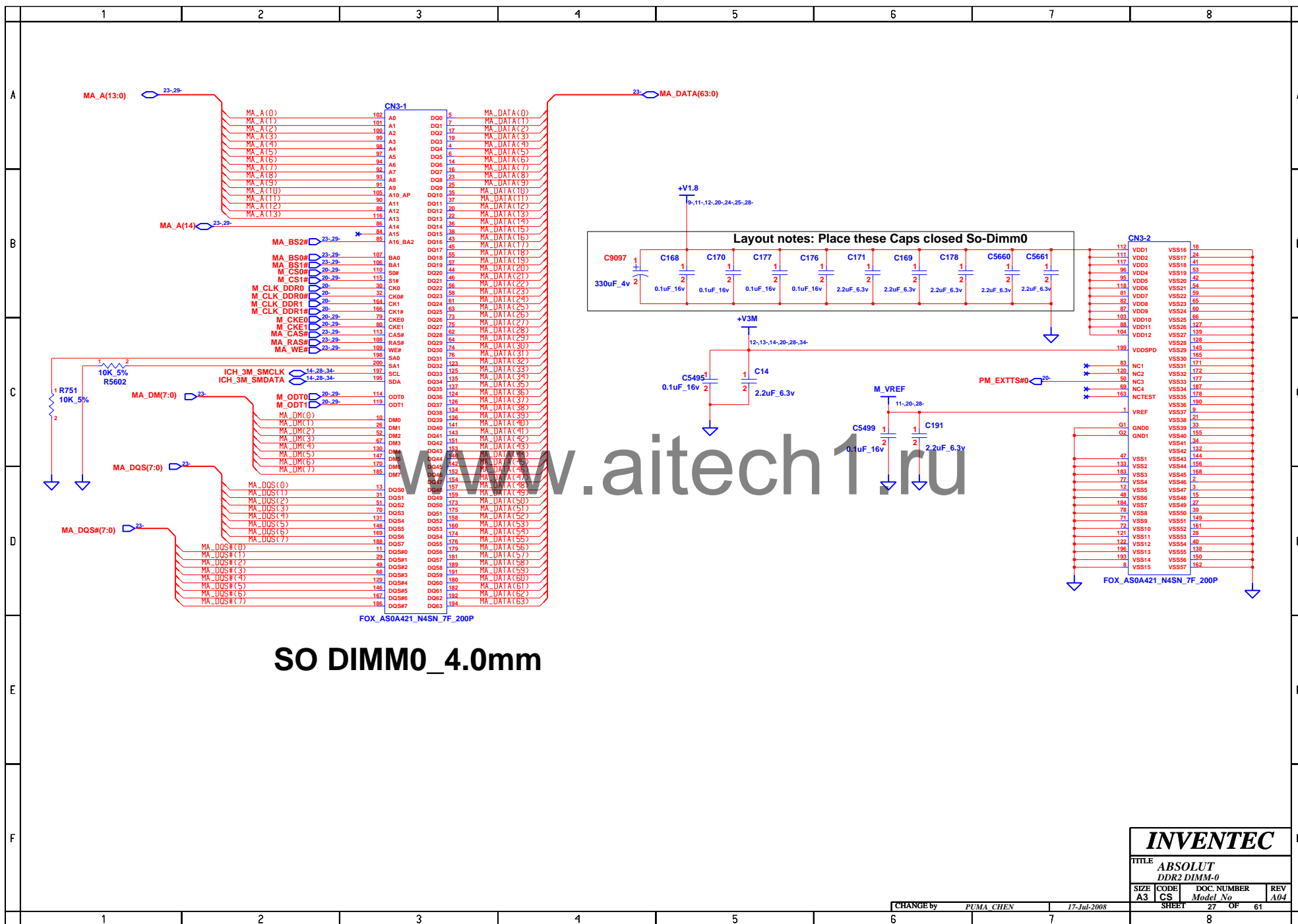
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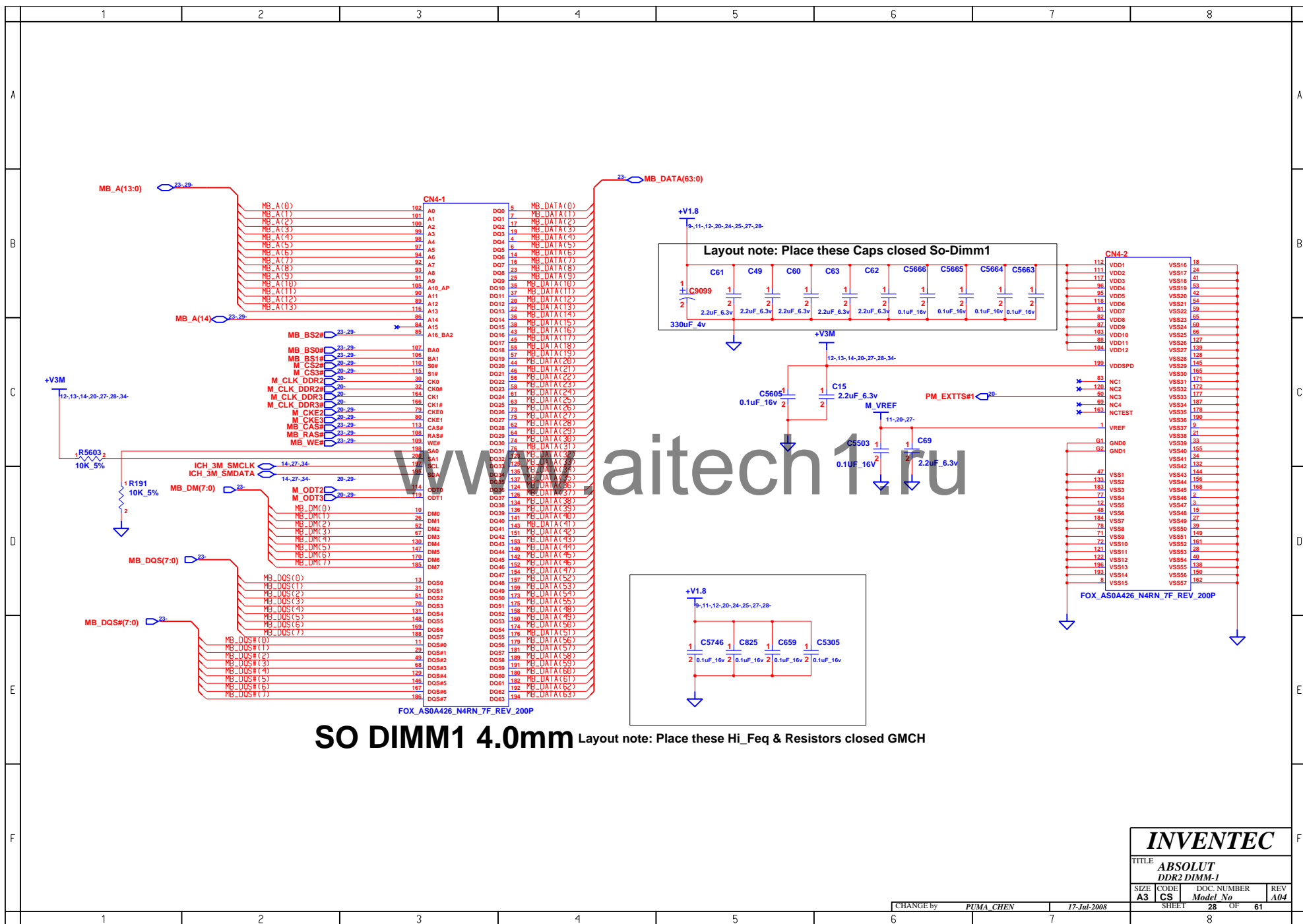
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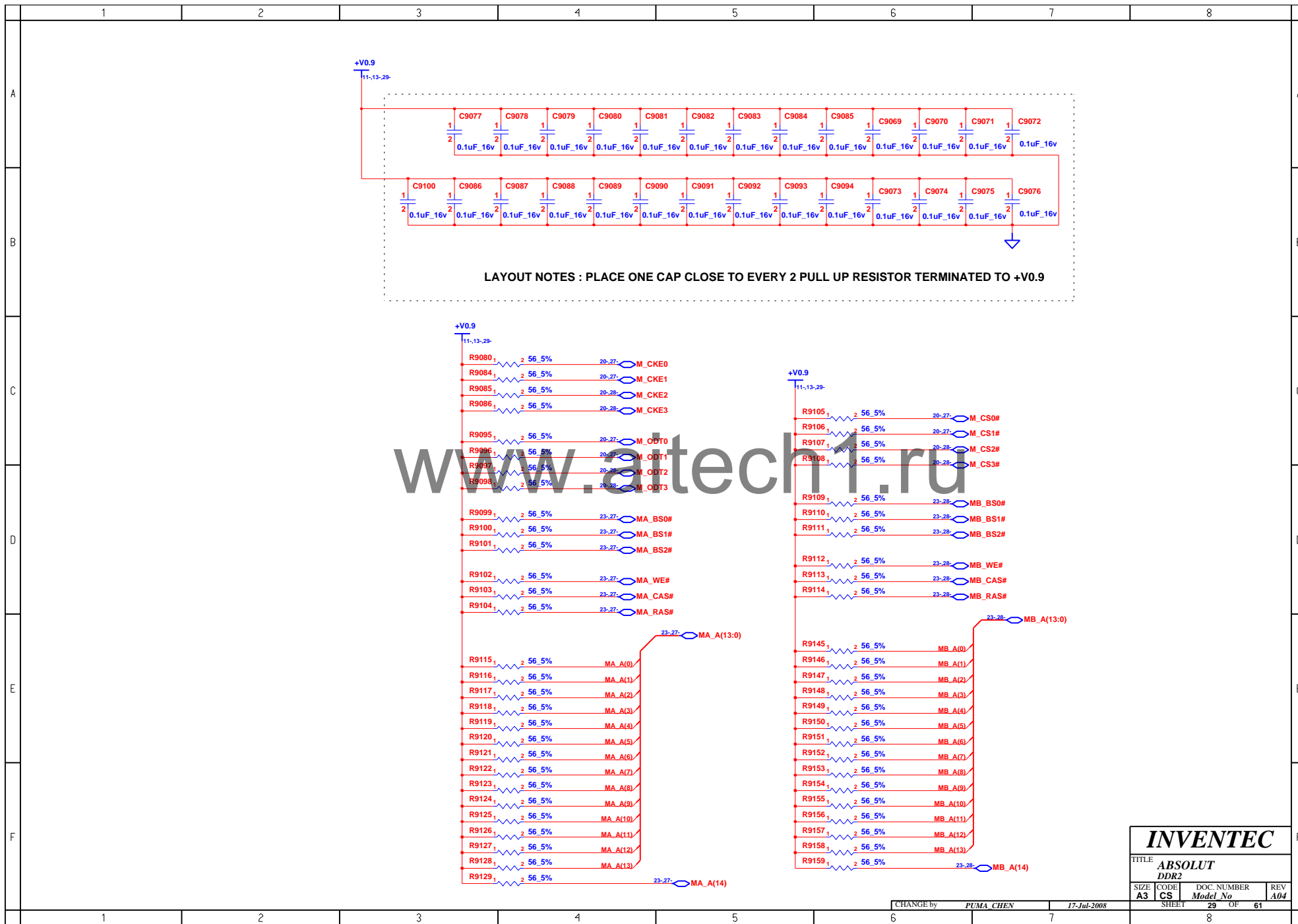
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DDR2 DIMM-0

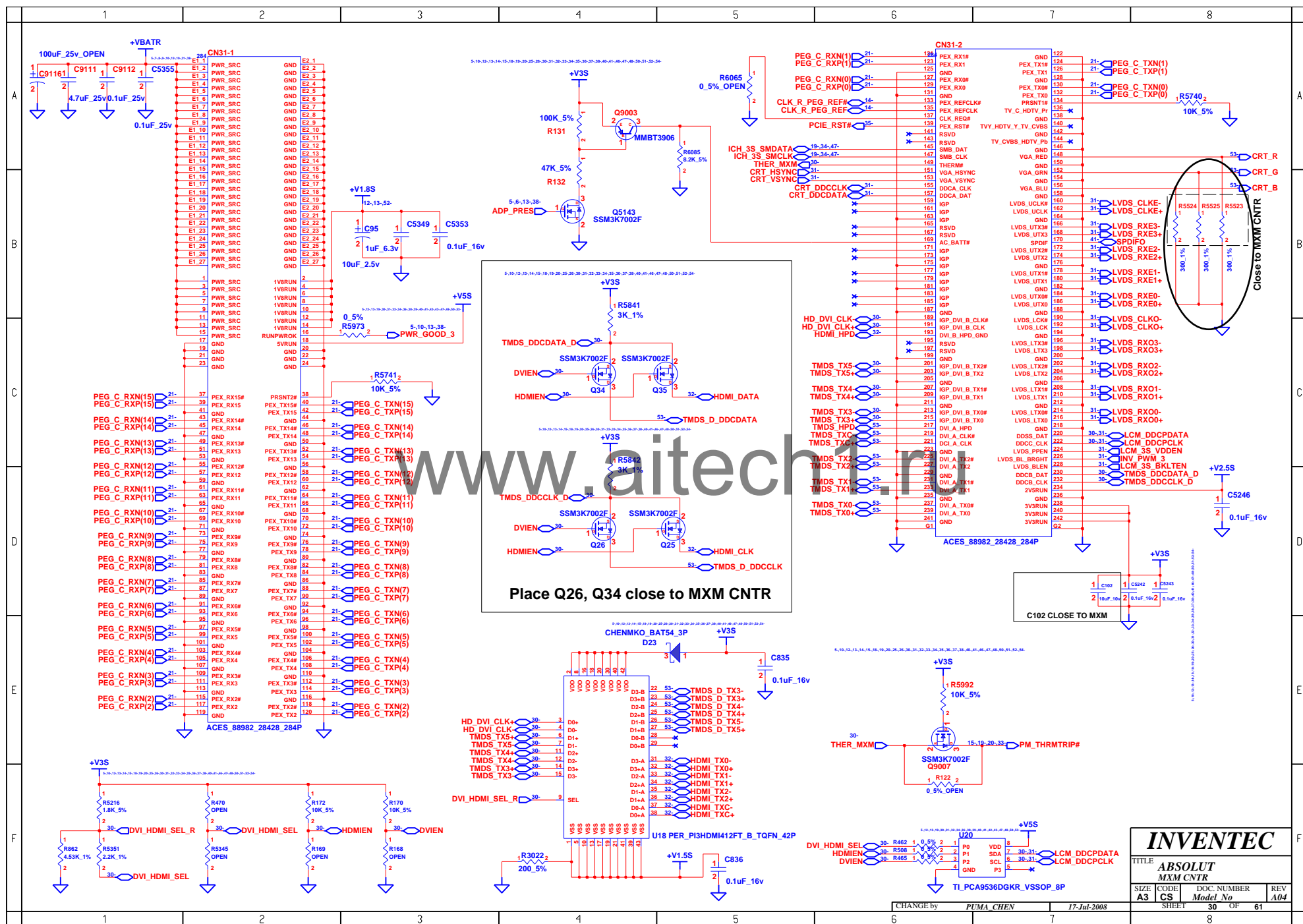
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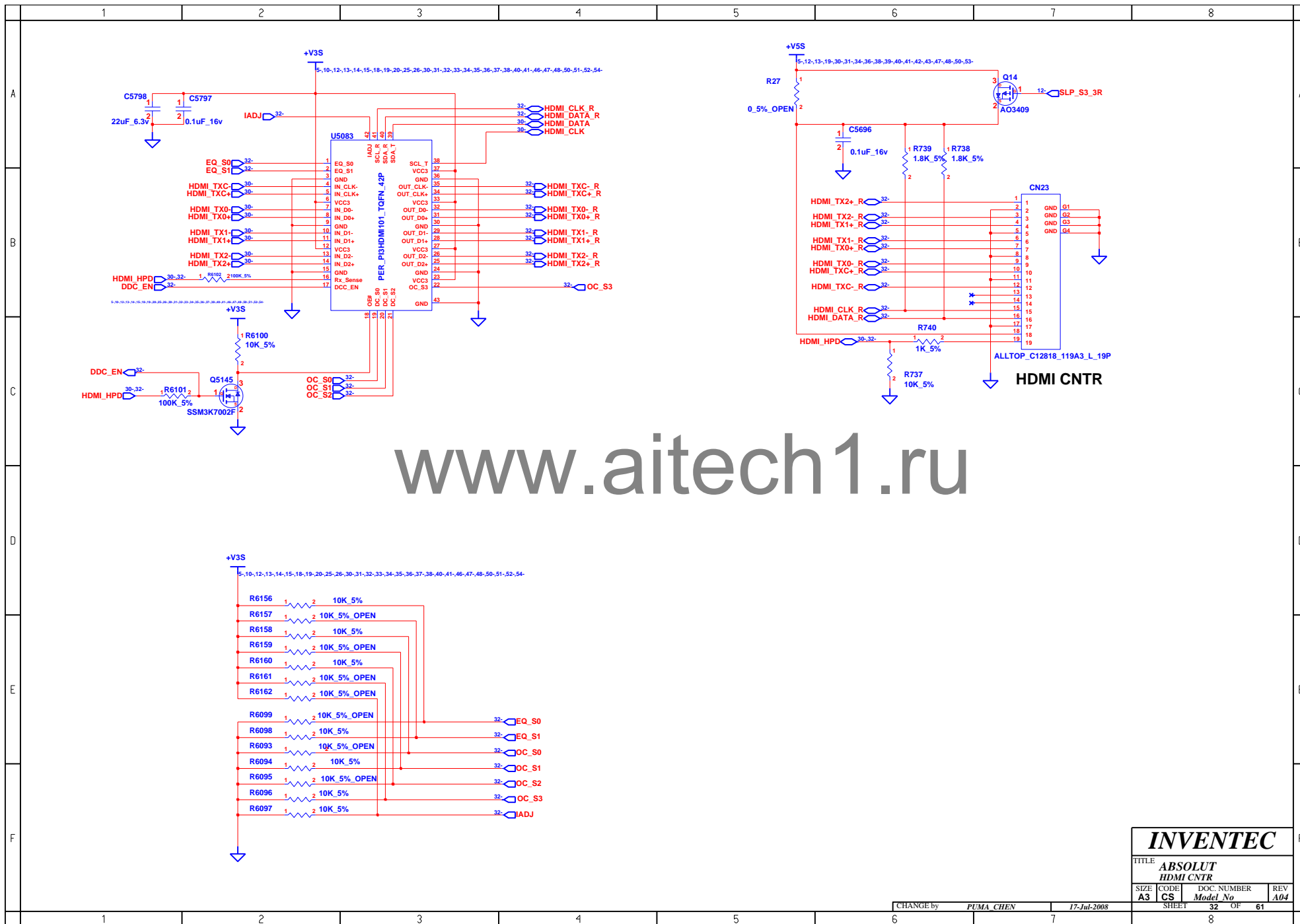
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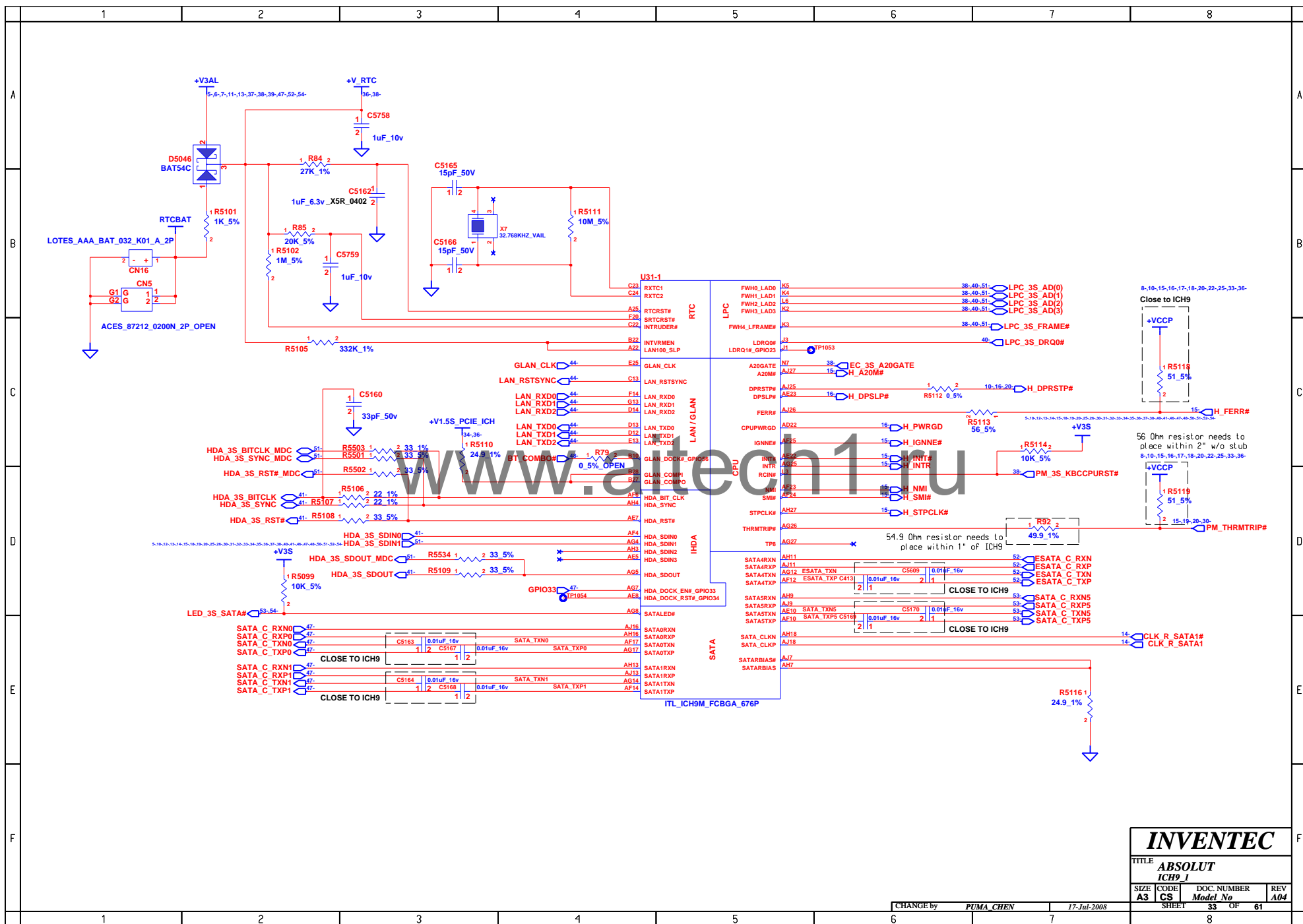


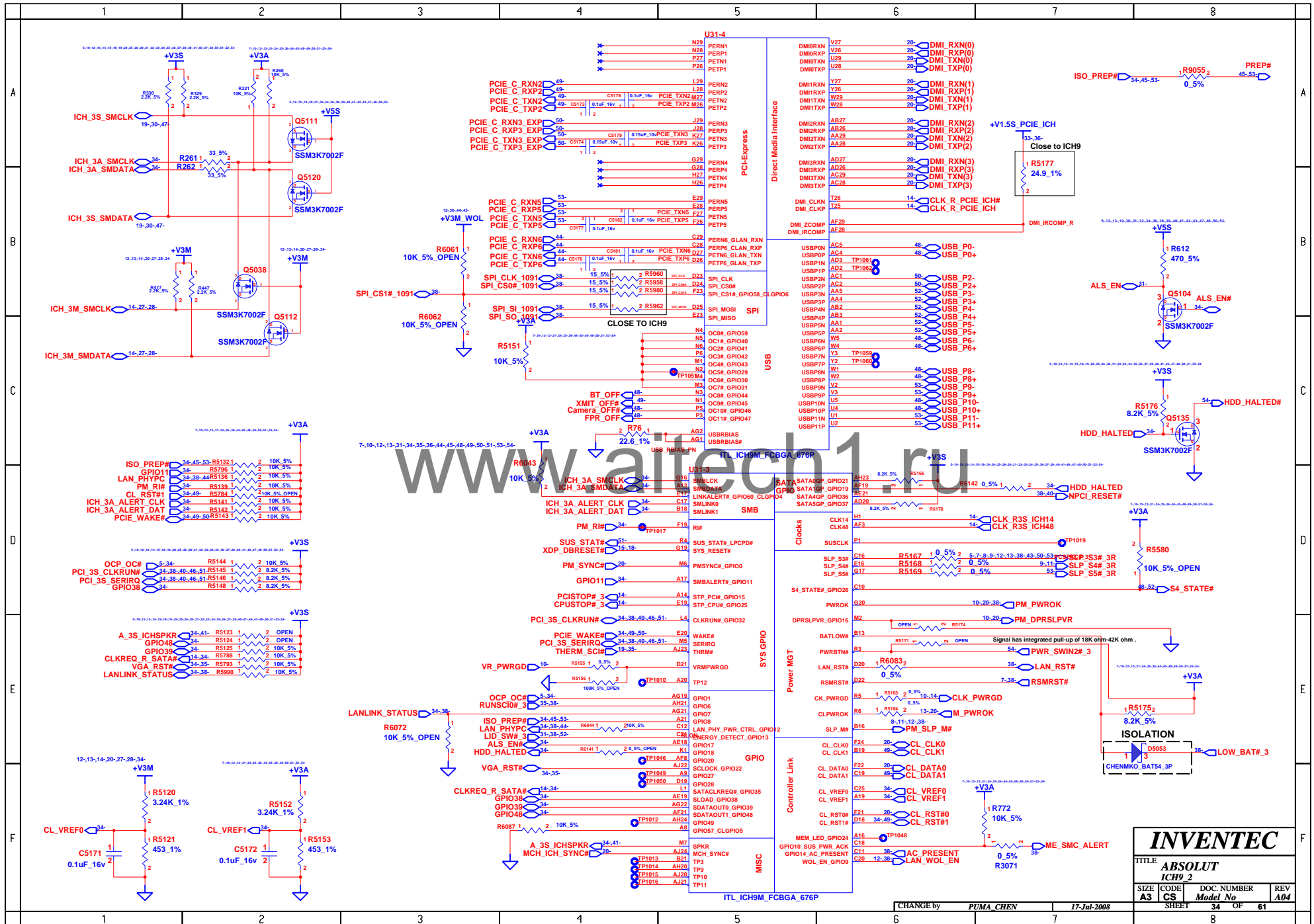


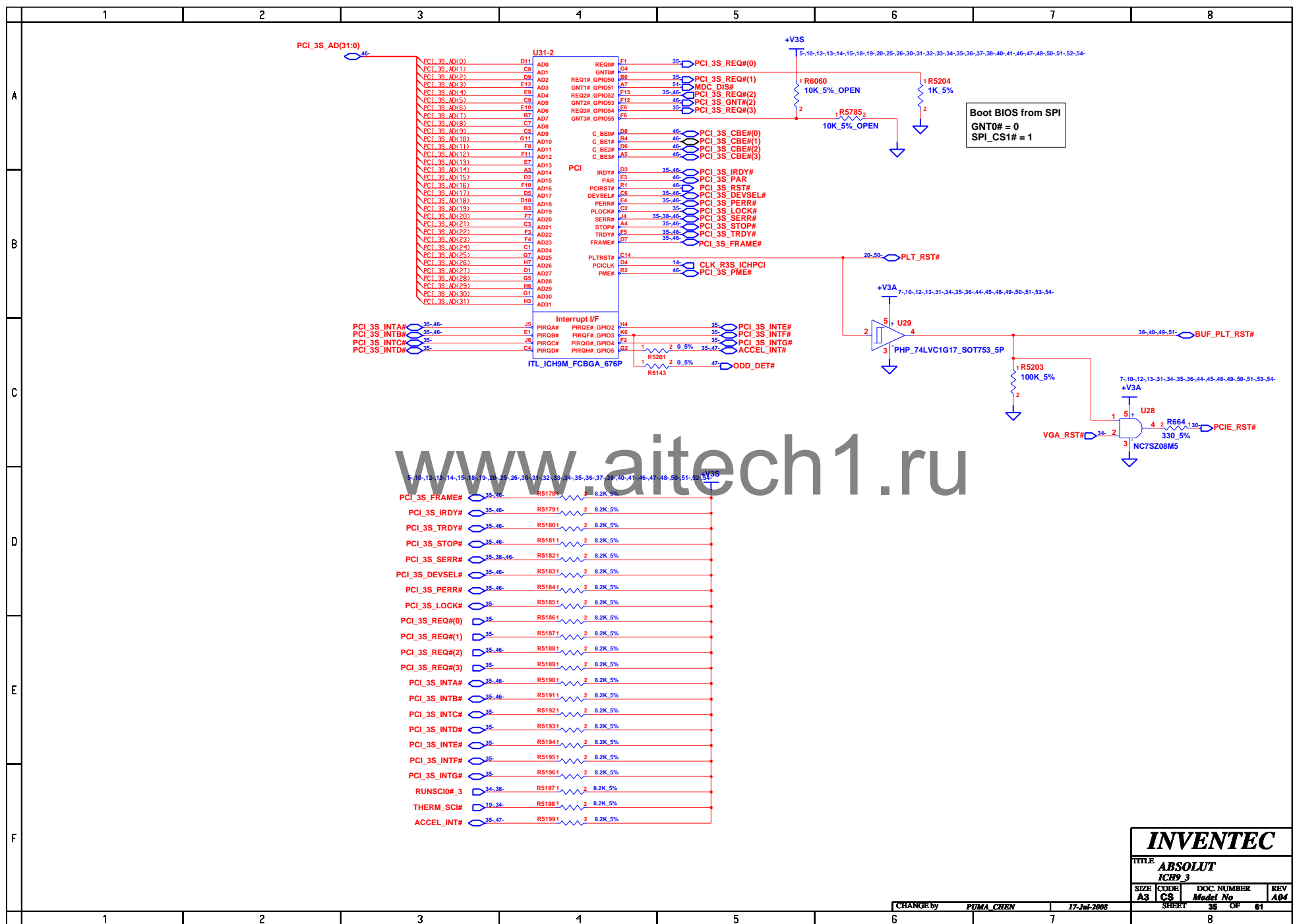


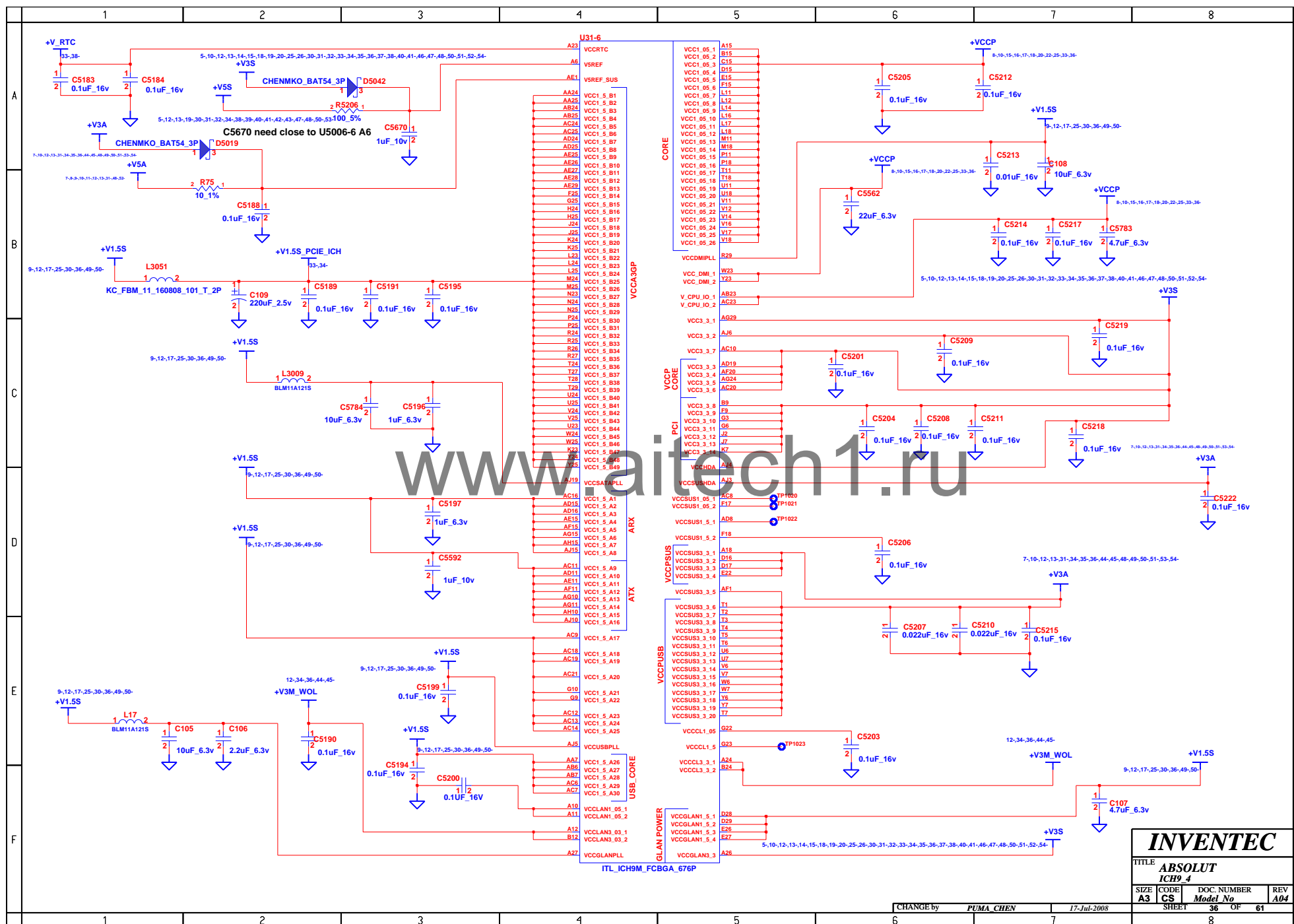


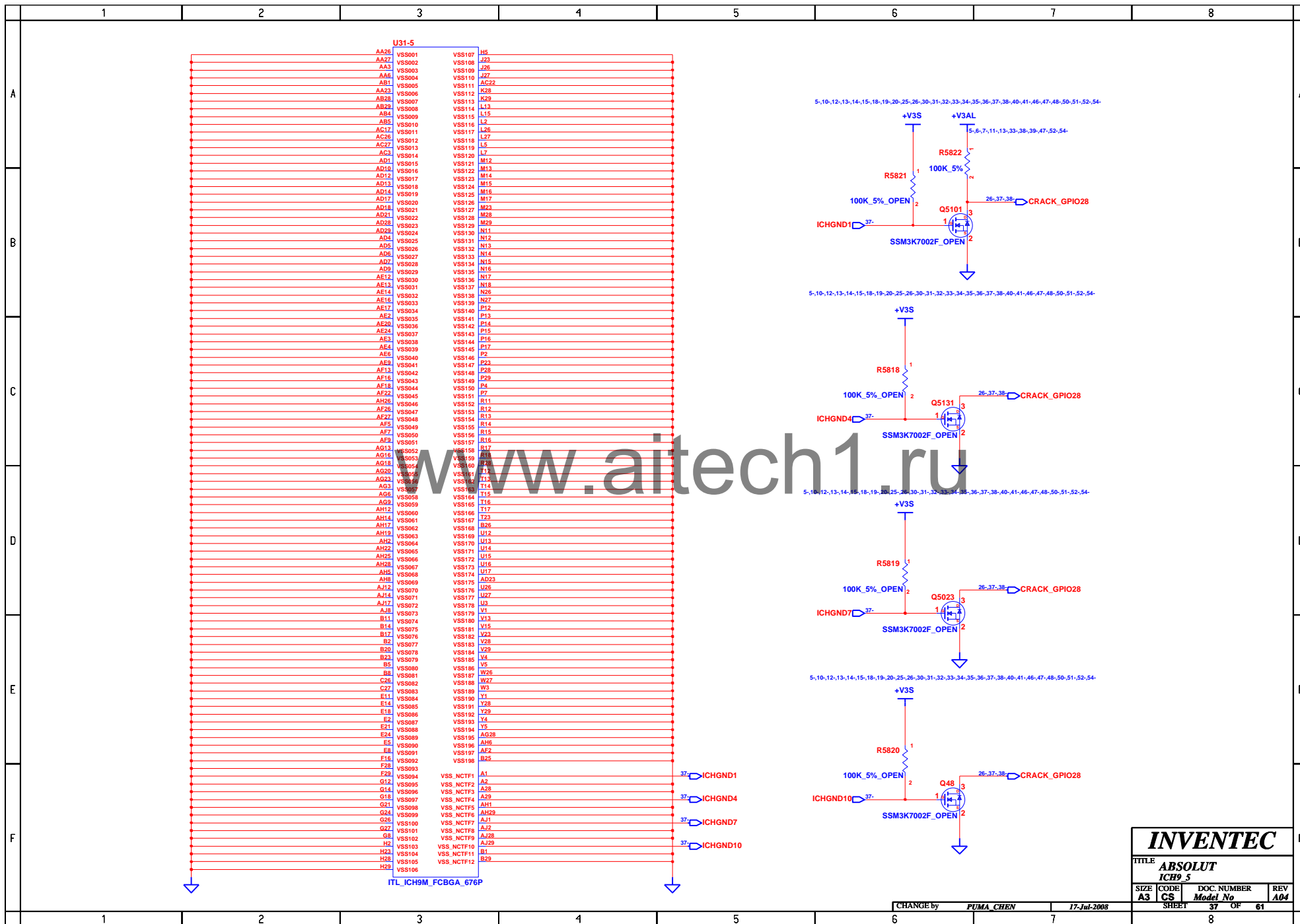
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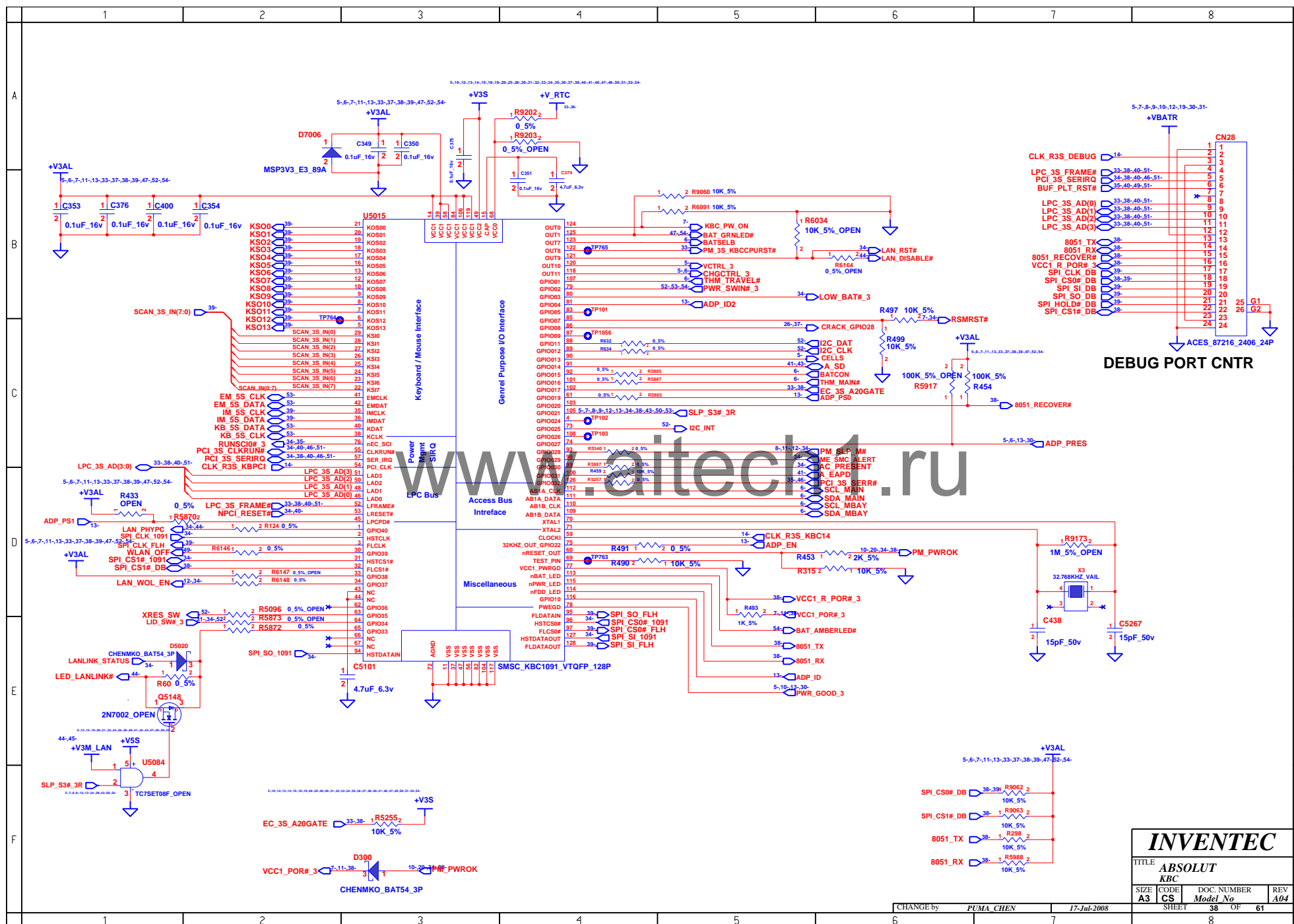


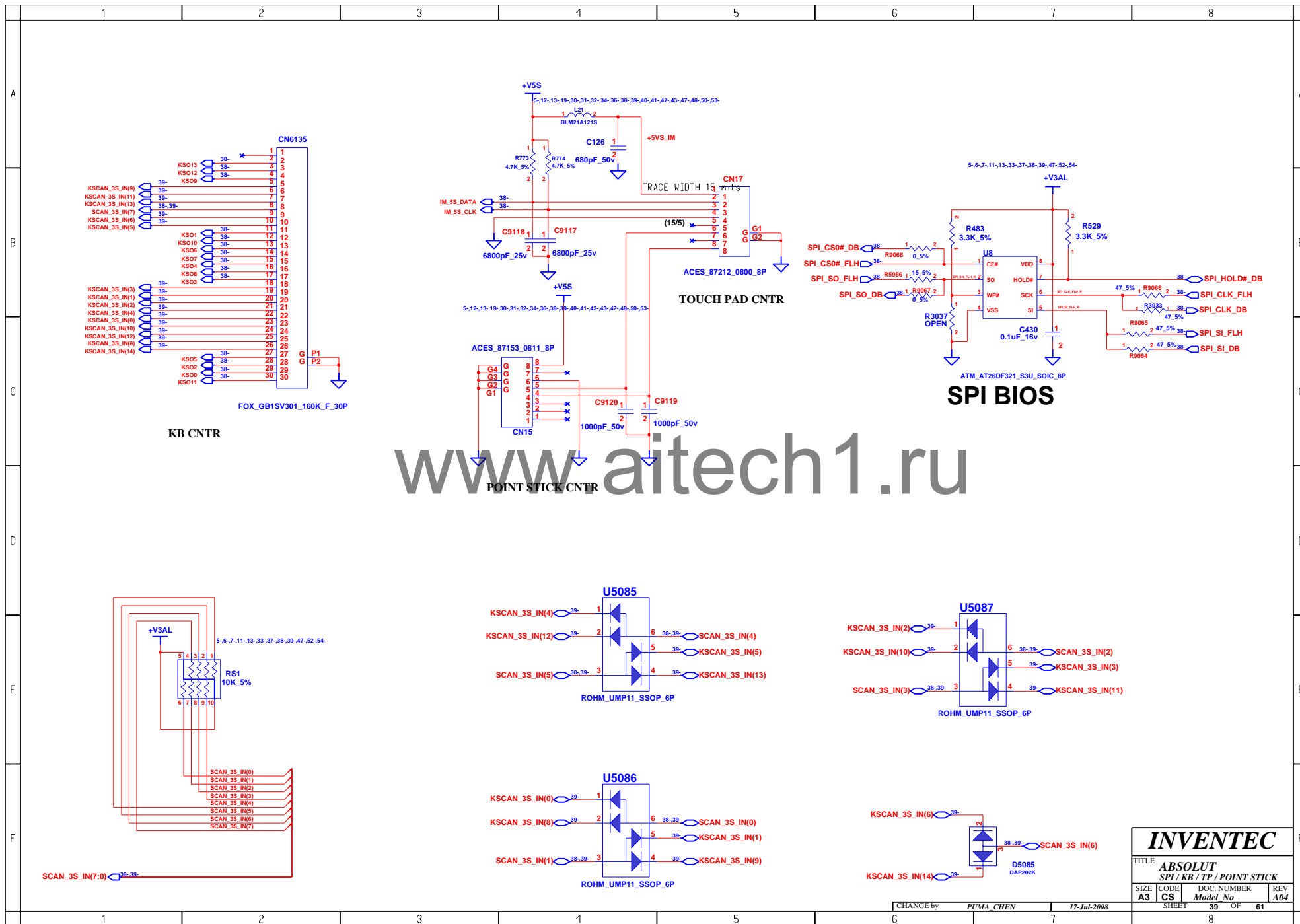




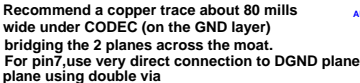




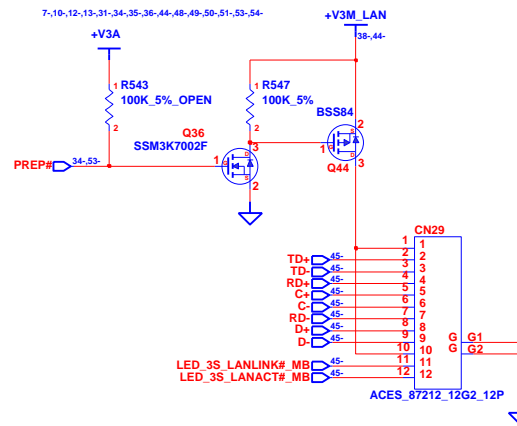
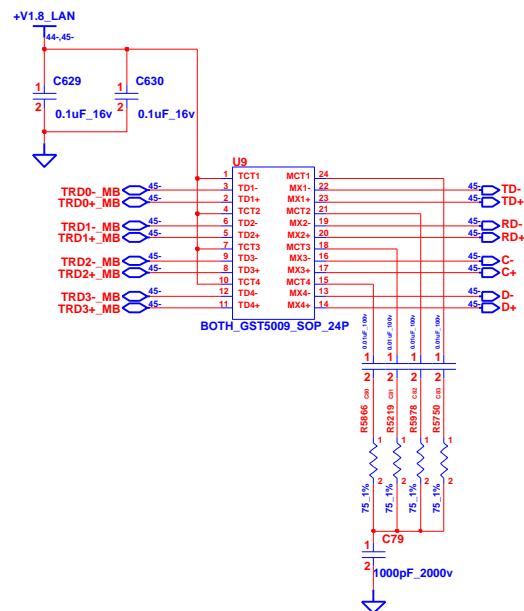
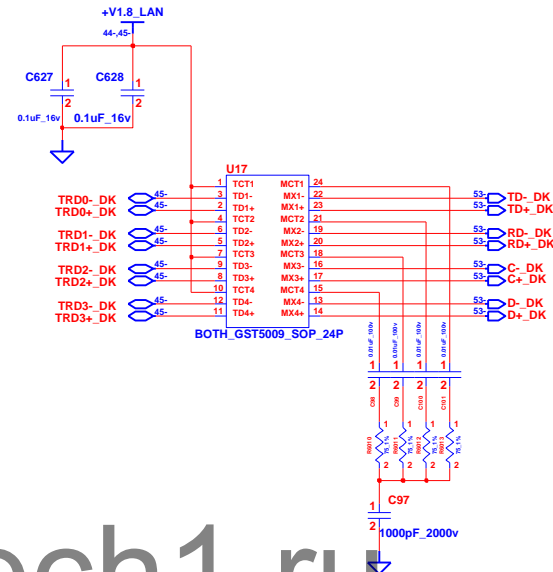
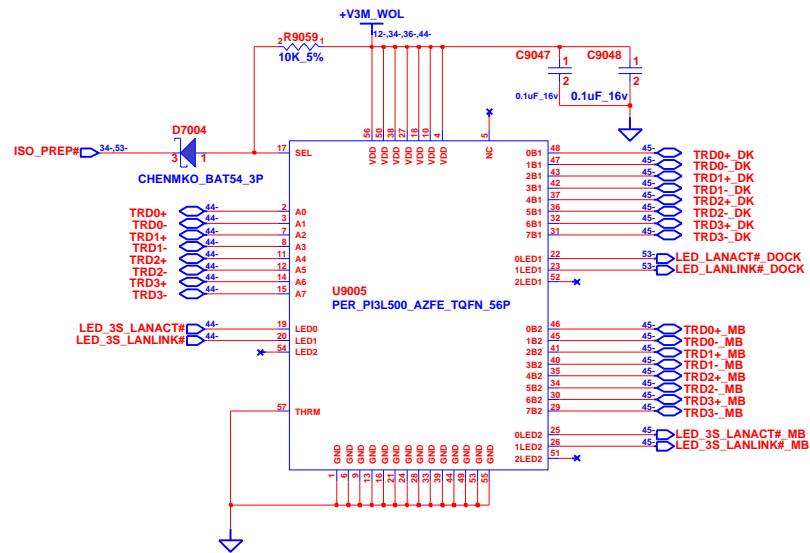




CS Model No
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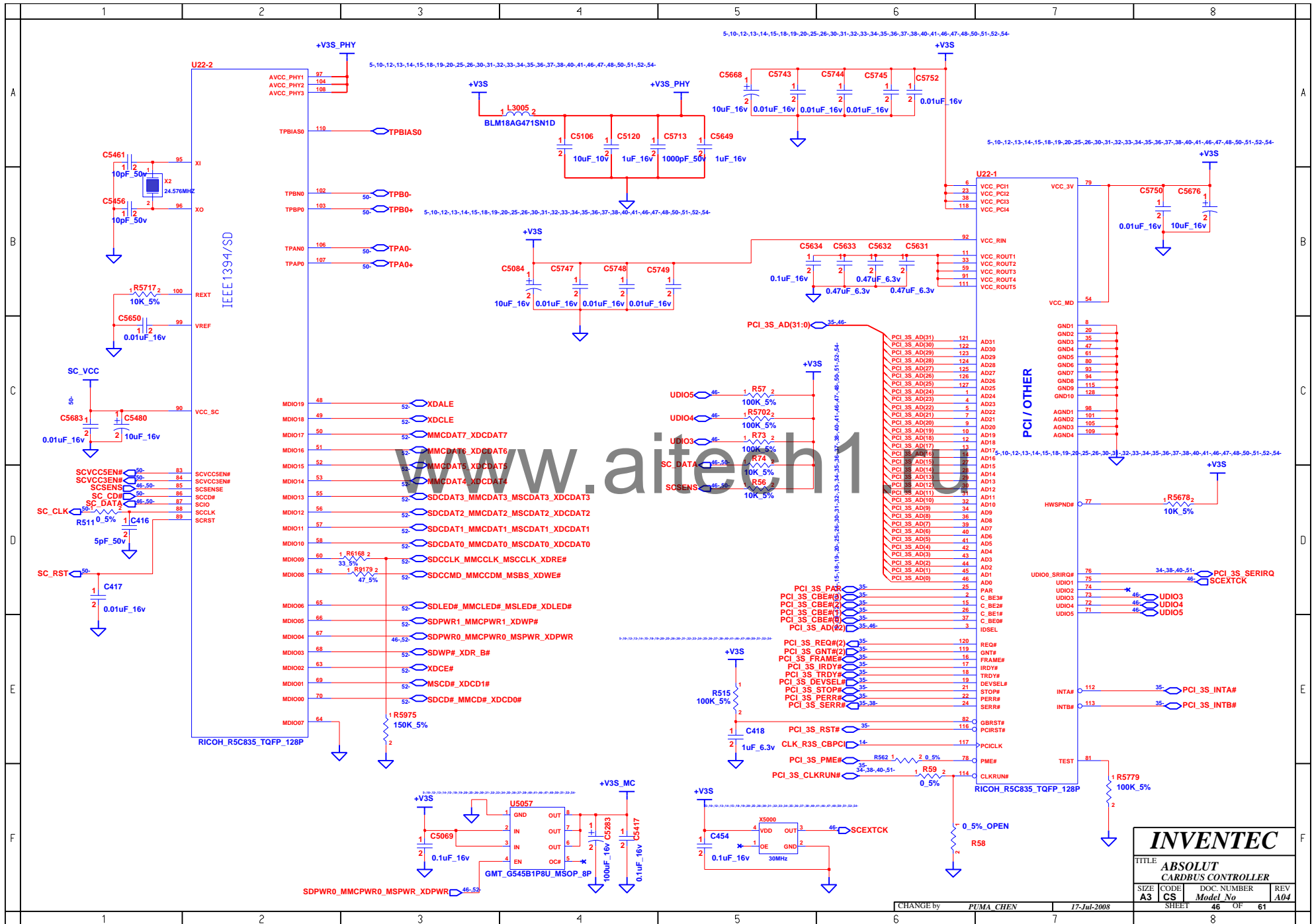
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RJ45 CNTR

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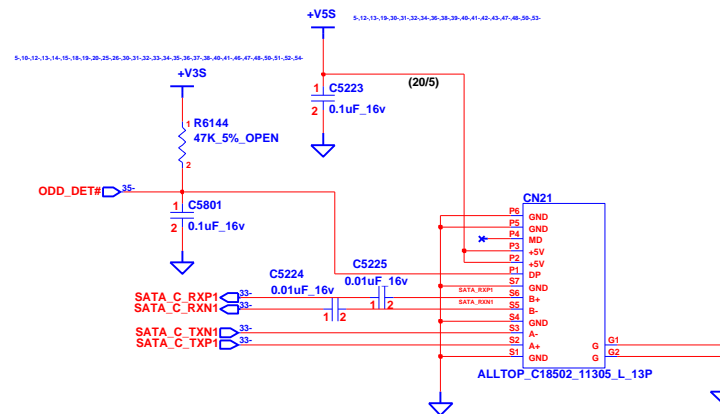
www.aitech1.ru



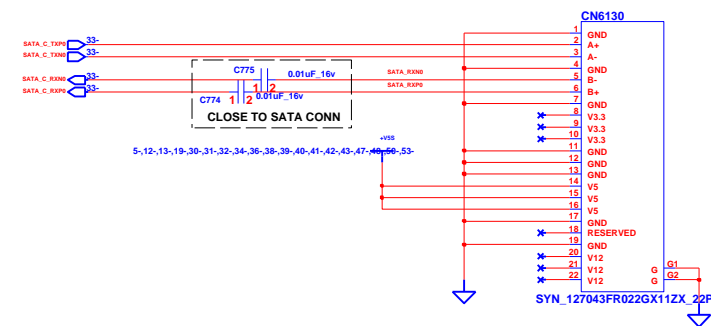
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A3	CS	Model No	A04
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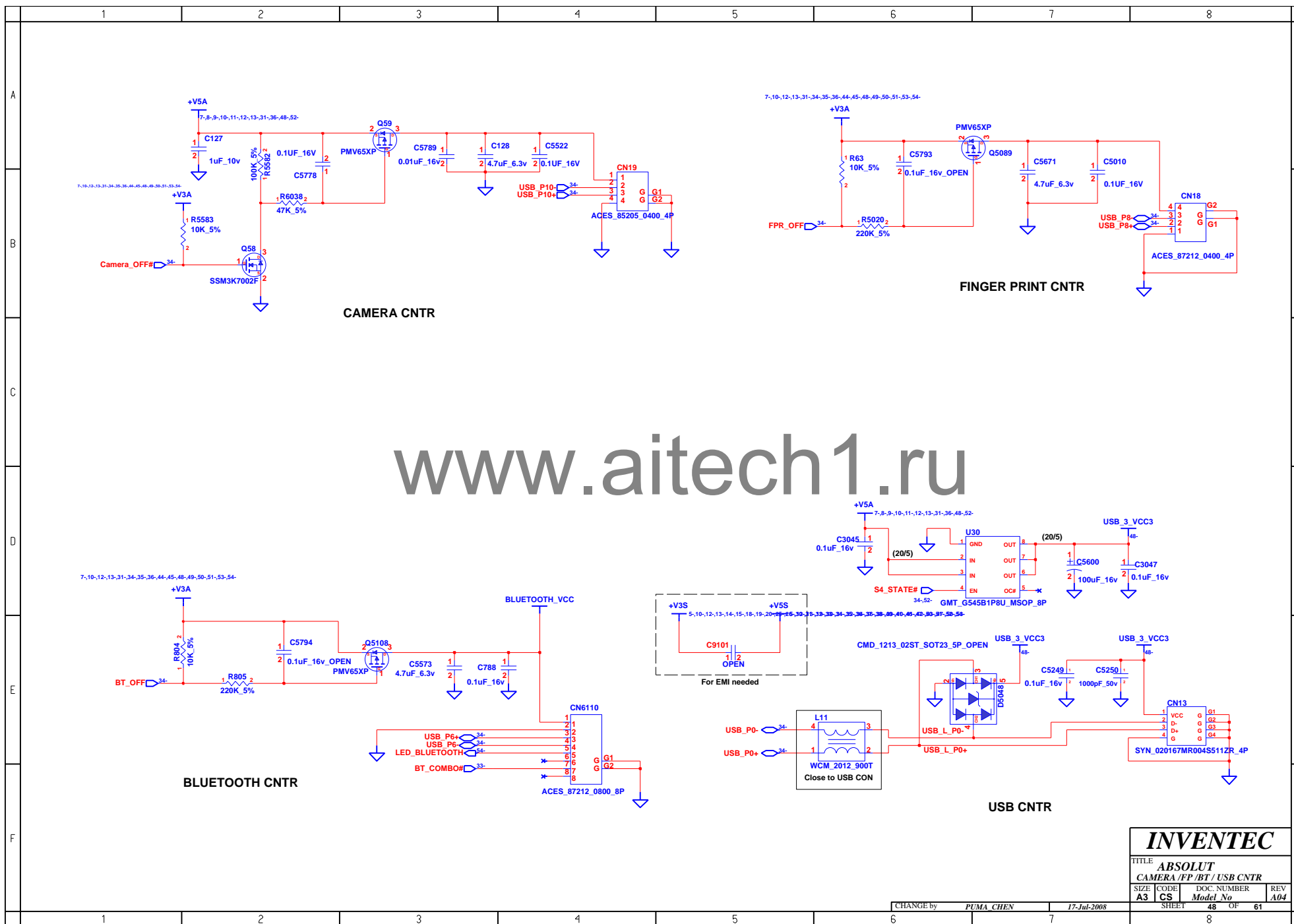
CHANGE by PUMA CHEN 17-Jul-2008



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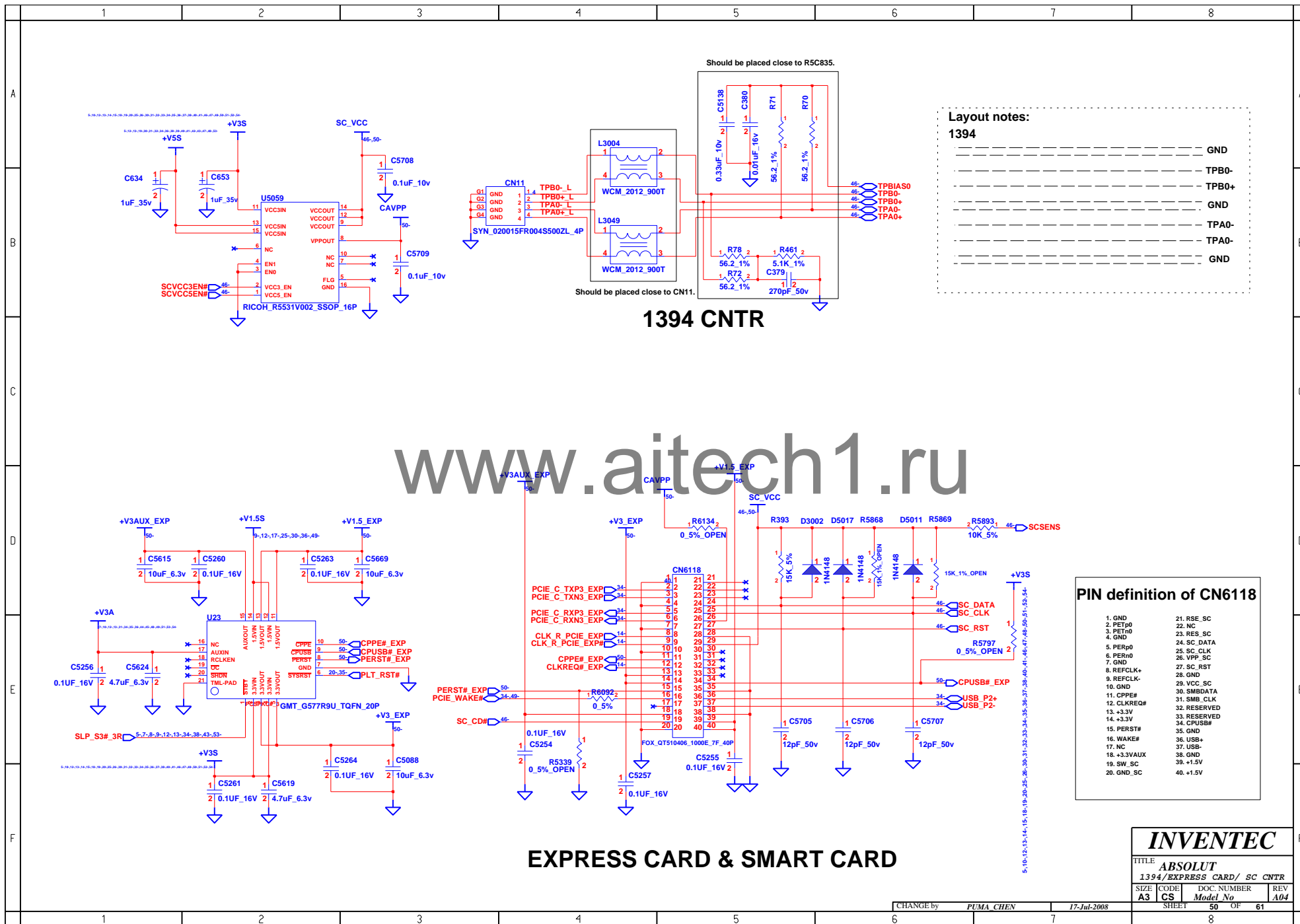
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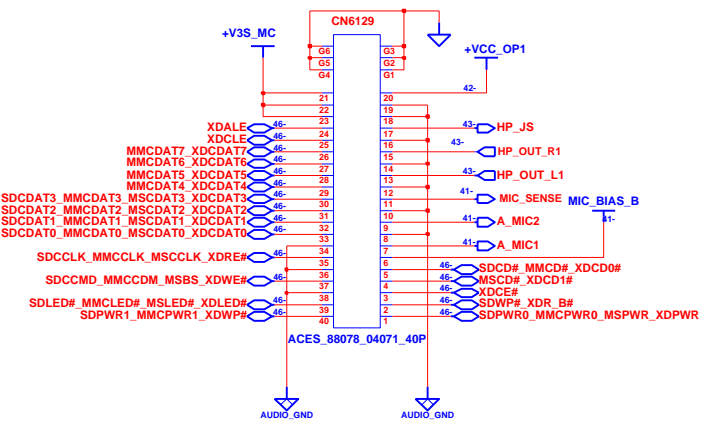
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SIZE	CODE	DOC. NUMBER	REV
<i>A3</i>	<i>CS</i>	<i>Model No</i>	<i>A04</i>



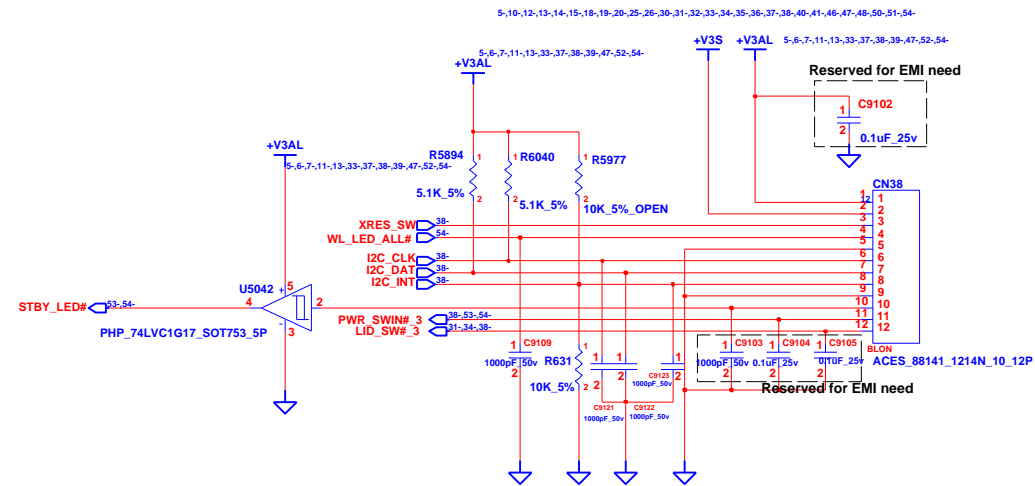


CS	Model No		
SHEET	49	OF	61

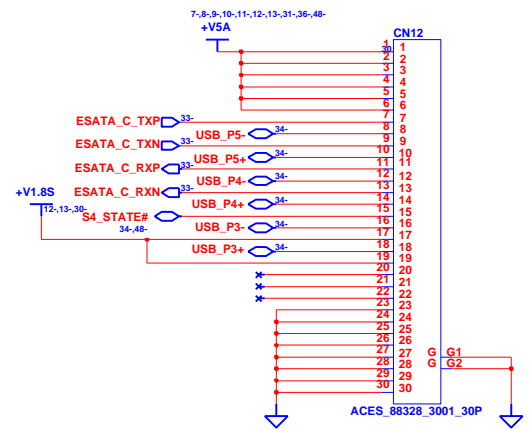




7IN1 MEDIA SOCKET / AUDIO JACK - BOARD CNTR



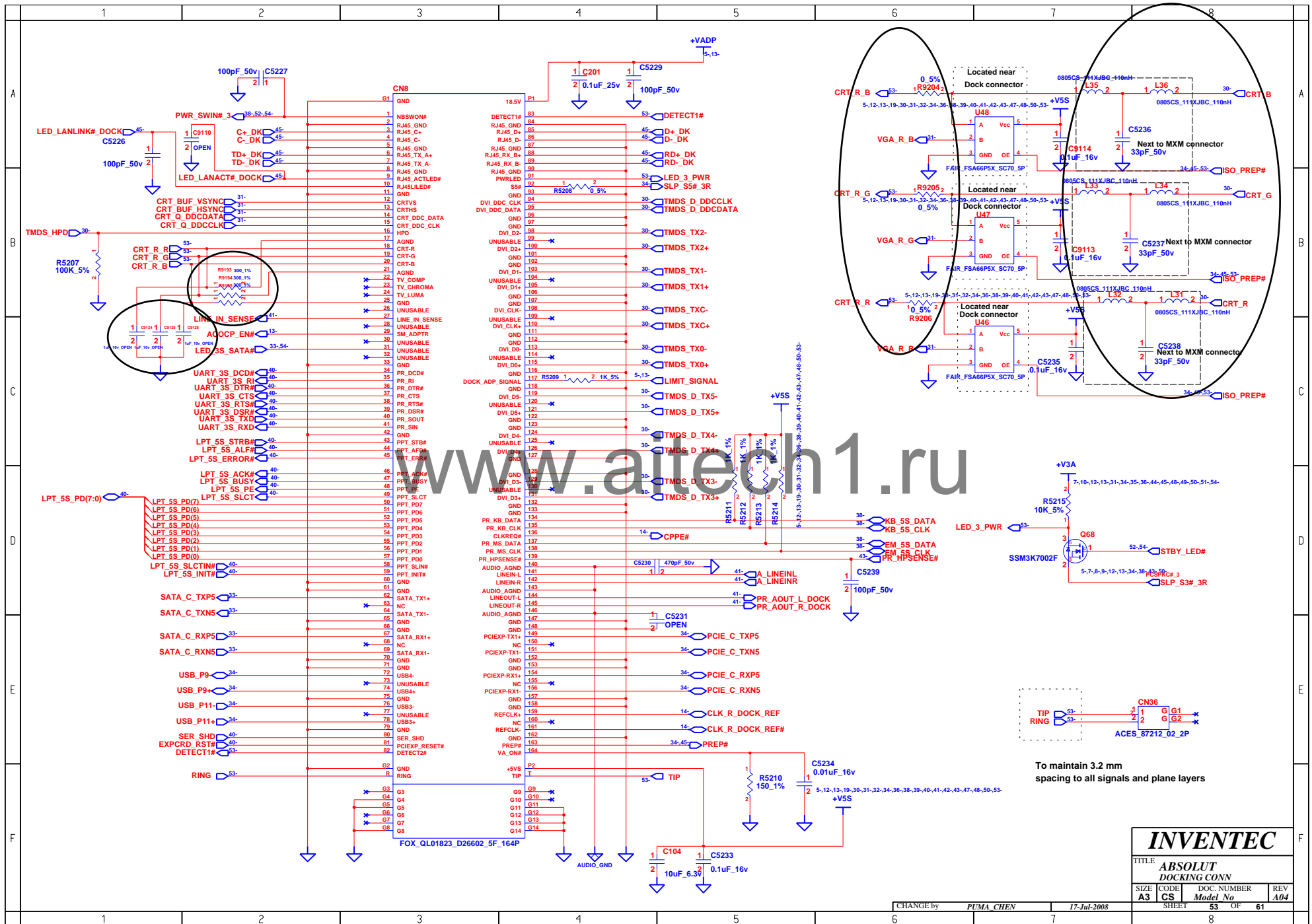
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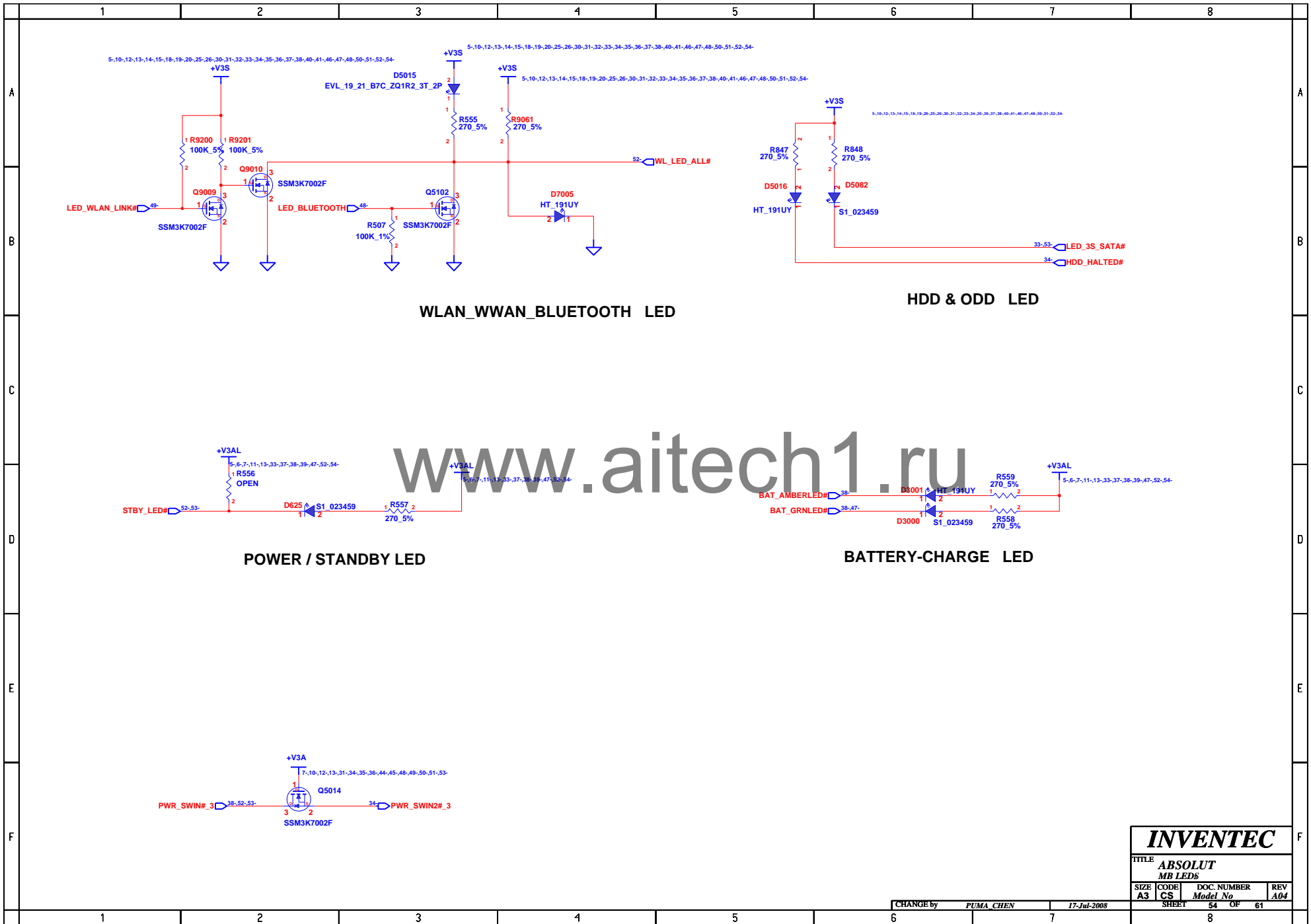


USB/ESATA - BOARD CNTR

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INVENTEC			
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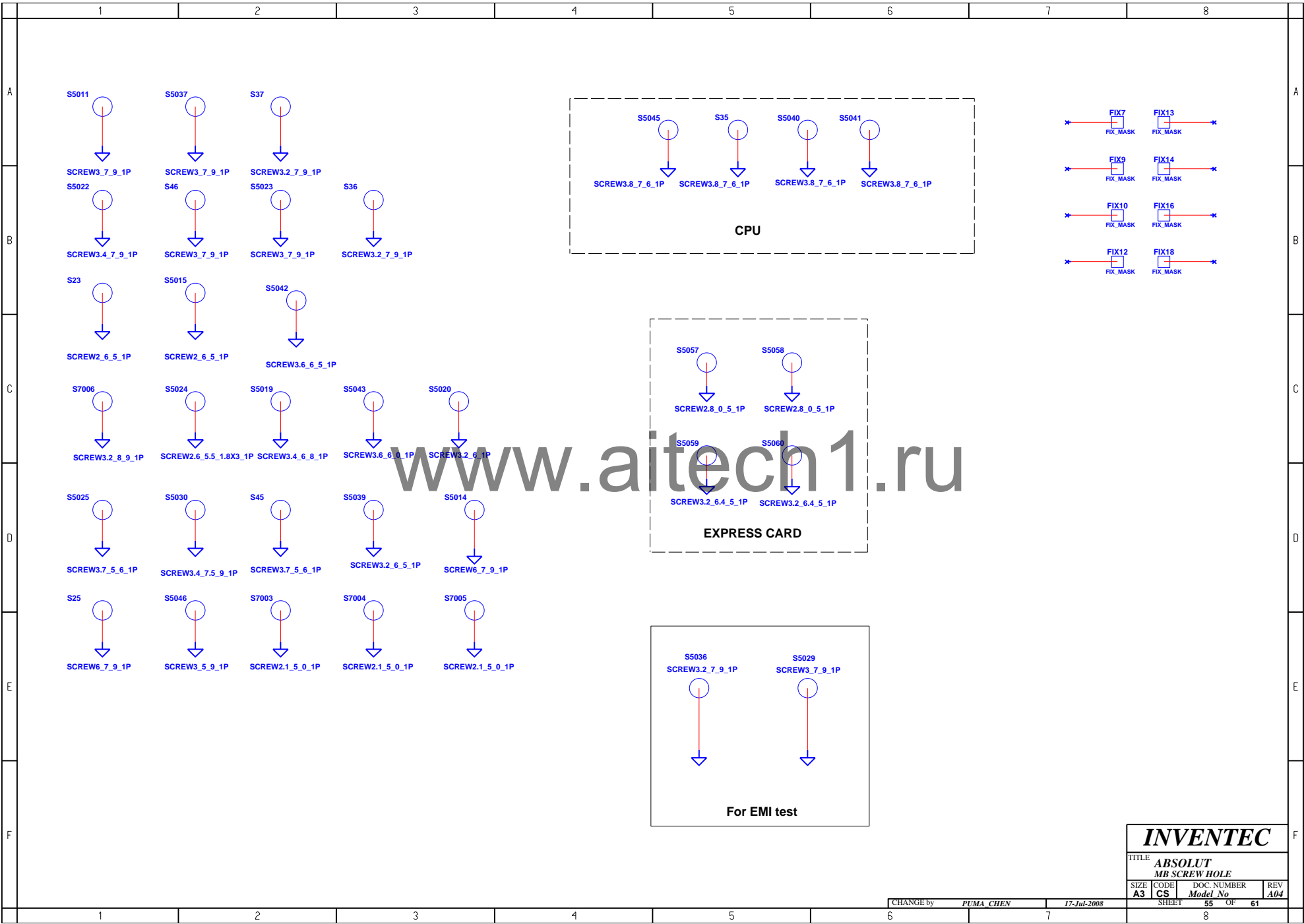


INVENTEC

TITLE ABSOLUT MB LEDs			
SIZE A3	CODE CS	DOC. NUMBER <i>Model No</i>	REV A04
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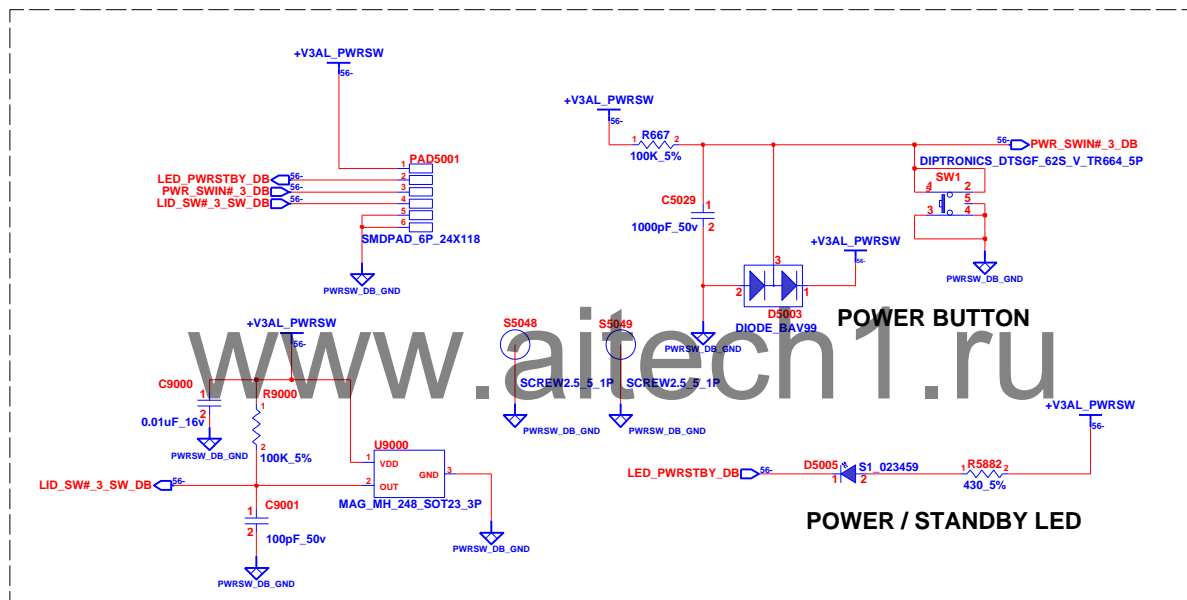
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TITLE
**ABSOLUT
MB SREW HOLE**

SIZE CODE DOC. NUMBER REV
A3 CS Model No. A04

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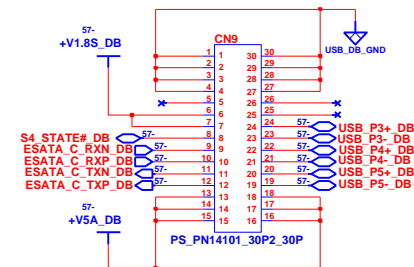
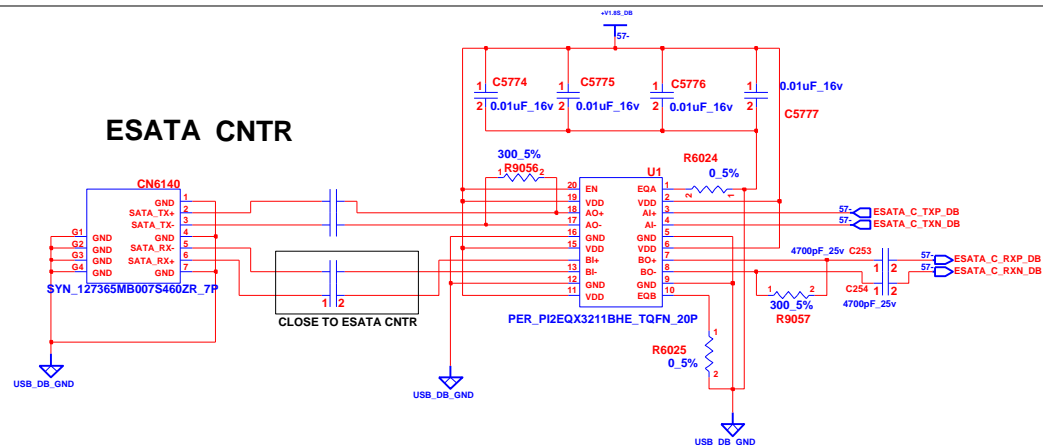


Daughter Board - Power Button

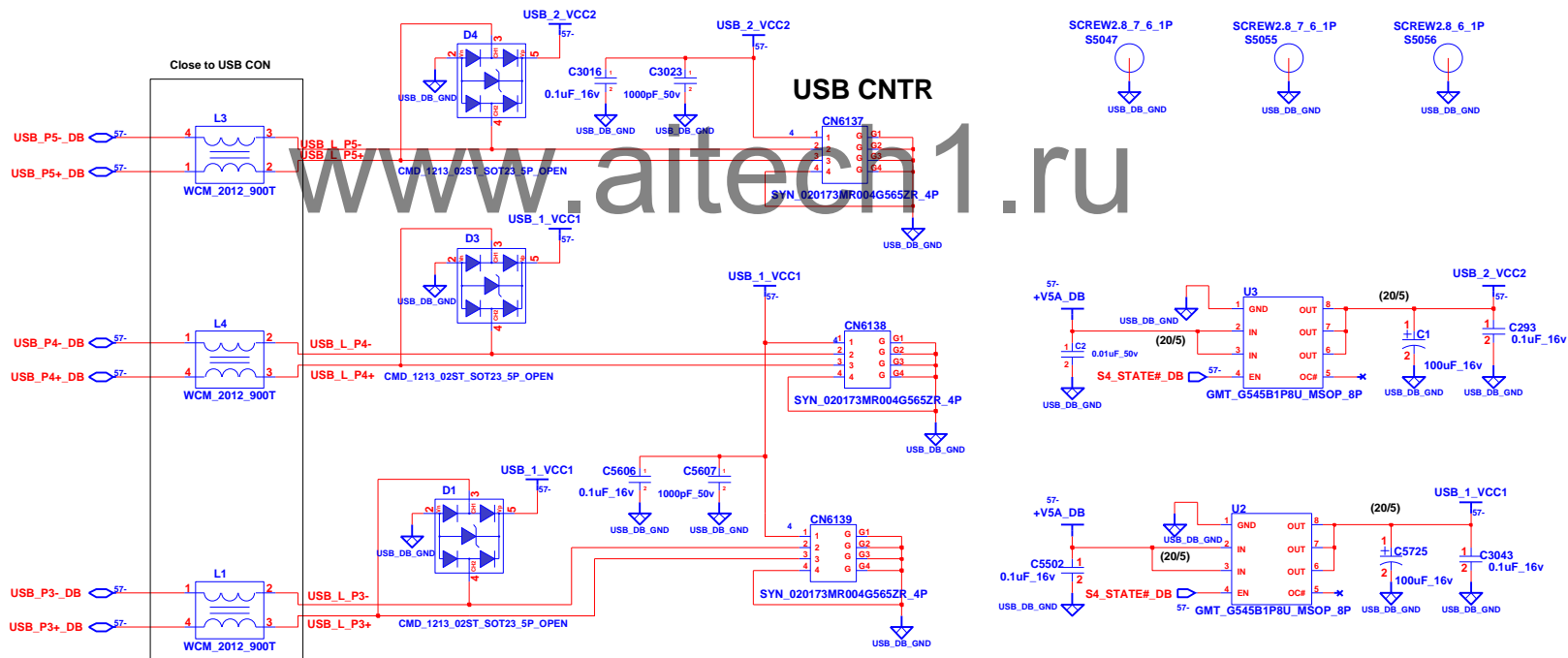
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SIZE A3	CODE CS	DOC. NUMBER Model No	REV A04
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ESATA CNTR



USB CNTR



Daughter Board - USB Port & eSATA

INVENTEC

TITLE ABSOLUT DB- USB/ESATA			
SIZE A3	CODE CS	DOC NUMBER Model No	REV A04

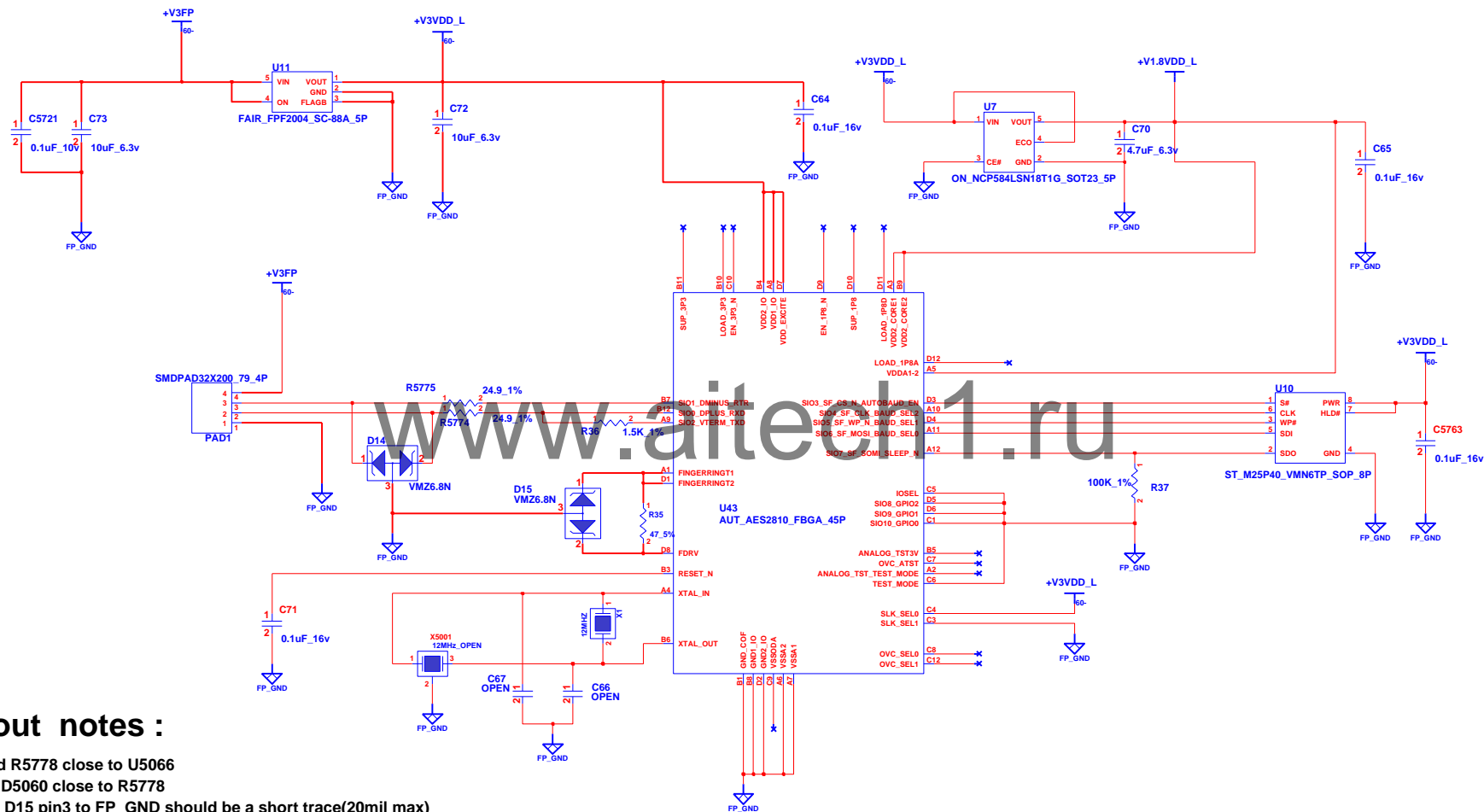
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B									B
C									C
D									D
E									E
F									F
	1	2	3	4	5	6	7	8	

INVENTEC			
TITLE ABSOLUT			
DB- MEDIA SOCKET/ AUDIO JACK			
SIZE	CODE	DOC. NUMBER	REV
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Layout notes :

1. Placed R5778 close to U5066
2. Place D5060 close to R5778
3. D14 & D15 pin3 to FP_GND should be a short trace(20mil max) using three via to connect to FP_GND

Daughter Board - Finger Print

INVENTEC

TITLE ABSOLUTE DB- FingerPrint			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV A04

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B									B
C									C
D									D
E									E
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